

# MV-D752-80

CMOS area scan camera



**Camera User's Manual**

REV: 1.1

photon focus

CAMERA  
Link

CE

## **MV-D752-80 User's Manual**

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Photonfocus, formed as a Spin-off from the Swiss Research Center for Electronics and Microtechnology (CSEM) in April 2001, is dedicated to making the latest generation of CMOS technology commercially available. Active Pixel Sensor (APS) and global shutter technologies enable high speed applications and applications with high picture contrast (120 dB) to be realized, while avoiding the disadvantages, e.g. image lag, of conventional logarithmic CMOS sensors. LinLog™ Technology was recognized with the Stuttgart Vision 2000 prize for innovation and, more recently, the Photonics Award of Excellence. With these technologies, blooming and smear belong to the past.

With the digital MV-D1024, MV-D752 and MV-D640 camera series, Photonfocus has proven that the image quality of modern CMOS sensors is now appropriate for demanding measurement and automotive applications. The MV-D1024 camera attains full frame rates of up to 150 fps with megapixel resolution; by using the Region Of Interest (ROI) feature, the frame rate can be increased to well over 1000 frames per second. The cameras can be supplied with either an LVDS (RS644) or a CameraLink digital interface.

The product range of Photonfocus is complemented by custom design solutions in the area of camera electronics and CMOS image sensors. Customer specific requirements, such as number of pixels, noise performance, dynamic range or sensitivity, can be implemented and optimized.

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## 1 Introduction

The CMOS mega-pixel Camera series MV-D752 from Photonfocus is aimed at demanding applications in industrial image processing and measurement. It offers an exceptionally high dynamic range of up to 120 dB with a resolution of 752 x 582 pixels and a full frame rate of up to 340 frames per second (MV-D752-160).

The CMOS camera series MV-D752, based on a CMOS sensor from Photonfocus, with 4 analog outputs, thus sets new standards in industrial image processing. The camera profits from the advantages of CMOS sensor technology over the more conventional CCD technology in the areas of e.g. blooming resistance, adjustable characteristics, selectable read-out window (Region Of Interest, ROI) and low energy consumption at high data rates. The global shutter permits high-speed applications in industrial image processing. In order to attain a higher dynamic range, the characteristics can be arbitrarily adjusted by the user between linear and logarithmic operation. Thus the LinLog™ technology is ideally suited to applications with high contrast.

The Photonfocus mega-pixel camera MV-D752-80 is available with LVDS (RS644) and CameraLink digital interfaces. The part codes of the various camera versions are shown in Table 1. Table 2 summarizes the camera properties.

To acquire images, the camera can be operated in master configuration, slave configuration or in trigger mode. In free-running mode, the camera (in master configuration) needs no external control signals to acquire images. The integration time and the read-out window (ROI) are pre-programmed in the camera via the configuration interface and can be changed by the user by means of the RS232 interface.

The slave configuration allows the user to control the camera externally with an external trigger signal, an external exposure signal or an external clock.

In trigger mode, the camera expects an external trigger signal defining the start of the exposure time, which is defined in the camera register.

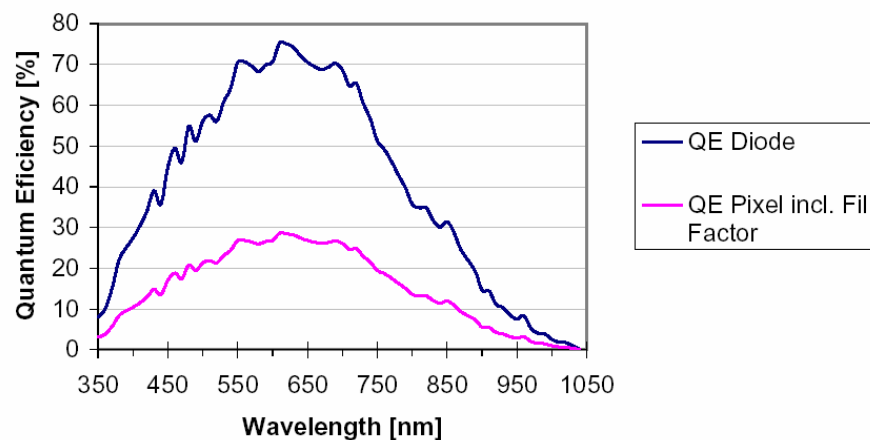
With its mega-pixel resolution, its high data rate as well as its high dynamic range and compact construction of only 55 mm x 55 mm x 50 mm (B x H x L), the MV-D752-80 is the perfect solution for applications with space restrictions, such as inspection stations or "Pick and Place" Machines, where, additionally, low energy consumption is beneficial. The versatility of the Photonfocus mega-pixel camera MV-D752-80 allows the optimization of the camera parameters for a given image processing application by the user. The camera parameters are continuously stored in an EEPROM and are loaded automatically at boot-up. The camera parameters can be set and stored in the EEPROM by using the API function library [SOFT] or the "PFRemote.exe" software [PFREMOTE], which are delivered with the camera and employ the RS232 protocol. **Low level programming of the module hardware independently of the API function library will not be supported by Photonfocus.**

**Table 1 : Part codes and order numbers for MV-D752-80 cameras**

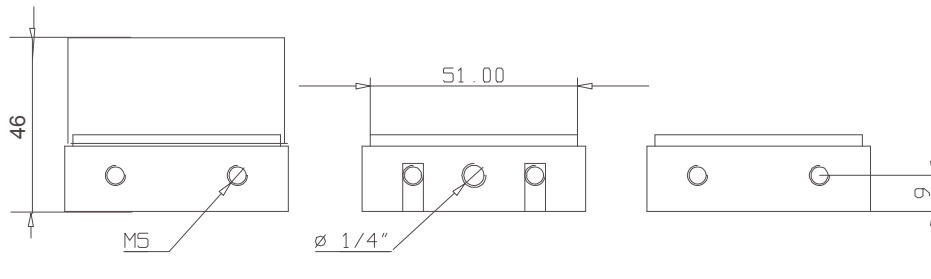
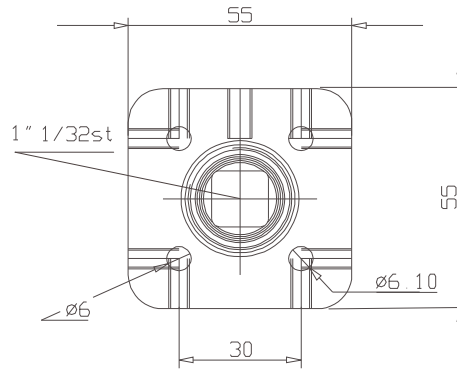
Interface	Part codes	Order numbers
CameraLink 8 bit	MV-D752-80-CL-8	60 20 50.003
LVDS (RS644) 8 bit	MV-D752-80-LV-8	60 20 50.004

**Table 2: Technical Data for the Photonfocus MV-D752-80 CMOS camera**

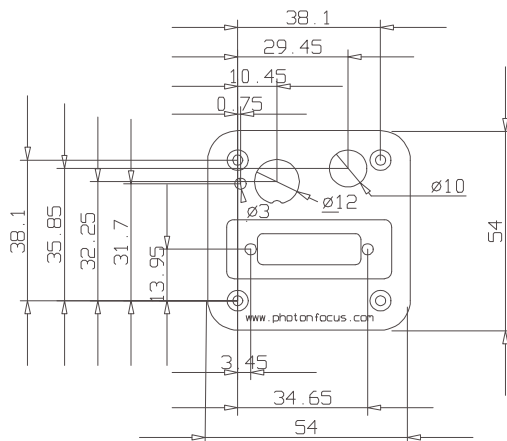
Technical Data for the Photonfocus MV-D752-80 CMOS camera	
Number of pixels	752 x 582
Pixel size	10.6 $\mu\text{m}$ x 10.6 $\mu\text{m}$
Optically active area	8.0 mm x 6.2 mm
Optical diagonal	10.12 mm $\rightarrow$ 2/3" optic
Objective mount	C-mount
Characteristic	Linear or LinLog™ adjustable
Full well capacity	200 ke <sup>-</sup>
Sensitivity	10 $\mu\text{J}/\text{m}^2/\text{LSB}$ @ 630 nm, 8 bit
Noise	< 0.5 Grey level standard deviation @ 8 bit
Fixed Pattern Noise	< 3 Grey level standard deviation @ 8 bit
Dynamic range in Linear Mode	> 48 dB @ 8 bit
Dynamic range in LinLog™ Mode	> 120 dB
Analog amplification	1 or 4
Spectral range	400 nm - 900 nm (see Fig. 1)
Optical Fill factor	35%
Data interface	LVDS and CameraLink
Data resolution	8 bit or 9 to 8 bit LUT
Internal Pixel clock	20.000 MHz
External clock rate CameraLink Interface	10.0 MHz to 20.0 MHz
External clock rate LVDS Interface	5.0 MHz to 20.0 MHz
Maximum frame rate	170 fps @ $T_{\text{int}} = 10 \mu\text{s}$
Shutter Type	global shutter
Exposure time	1 $\mu\text{s}$ - 0.5 s in steps of 50 ns
Configuration interface	RS232 Standard, 9600 baud, 1 Start bit, 1 Stop bit, no Parity bit
Voltage supply	+5V DC +/- 10%
Power consumption	2 W
Dimensions	55 mm (B) x 55 mm (H) x 50 mm (L)
Weight	200g
CE Test (see Appendix G)	EN 61000-6-3 : 2001 EN 61000-6-2 : 2001


**Fig. 1: Quantum efficiency as function of wavelength**

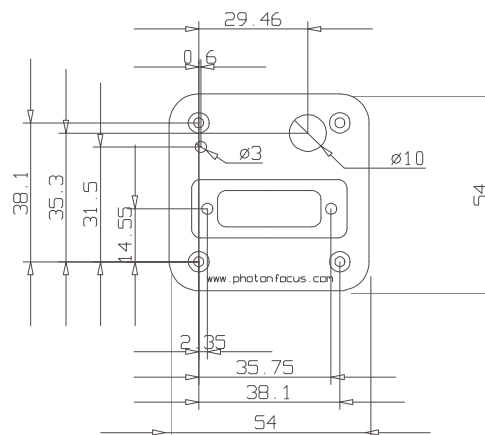
## 2 Mechanical Dimensions



Interface Camera Link



Interface LVDS



The Front plate is compatible with the Microbench System of LINOS AG ([www.linoss.de](http://www.linoss.de)) [MB2002].

### 3 Interface pin assignments

The CMOS camera series MV-D752 is available with a CameraLink interface in the base configuration or an LVDS (RS644) interface. The signal definitions, the bit allocations and the signal level of the CameraLink standard are described in [CLO2000]. Detailed information about the LVDS (RS644) standard is given in [LOM2000].

#### 3.1 CameraLink Interface

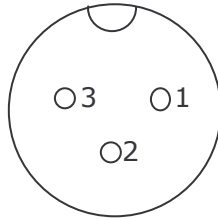
The CameraLink Interface has a socket with signals for data transfer and control of the camera functions as well as a socket for the voltage supply. The socket pin assignments for data and control signals are defined in the CameraLink Standard [CLO2000]. The socket assignment is shown in Table 3, the assignment of the data bits of the 8-bit taps 0 and 1 are shown in Table 5 and Table 6. The assignment of the pixels of the sensor to the sensor and camera taps are shown in the Fig. 3. The subminiature connector Binder Series 712 is used for current supply. The order number for the camera socket is 09-0408-90-03 (see Table 4 und Fig. 2). A plug (order number 99-0405-00-03) is necessary to connect the camera.

**Table 3: Pin assignments for the MDR26 socket of the CameraLink Interface**

PIN	I/O	Name	Description
1	PW	SHIELD	Shield
2	O	N_XD0	Negative LVDS Output, CameraLink DataD0
3	O	N_XD1	Negative LVDS Output, CameraLink DataD1
4	O	N_XD2	Negative LVDS Output, CameraLink DataD2
5	O	N_XCLK	Negative LVDS Output, CameraLink Clock
6	O	N_XD3	Negative LVDS Output, CameraLink DataD3
7	I	P_SERTOCAM	Positive LVDS Input, Serial Communication to the camera
8	O	N_SERTOFG	Negative LVDS Output, Serial Communication from the camera
9	I	N_CC1	Negative LVDS Input, External Trigger signal EXSYNC
10	I	P_CC2	Positive LVDS Input, External clock for Slave mode MCLK
11	I	N_CC3	Negative LVDS Input, Exposure control EXPOSURE
12	I	P_CC4	Positive LVDS Input, Control signal CONTROL <not used>
13	PW	SHIELD	Shield
14	PW	SHIELD	Shield
15	O	P_XD0	Positive LVDS Output, CameraLink DataD0
16	O	P_XD1	Positive LVDS Output, CameraLink DataD1
17	O	P_XD2	Positive LVDS Output, CameraLink DataD2
18	O	P_XCLK	Positive LVDS Output, CameraLink clock
19	O	P_XD3	Positive LVDS Output, CameraLink DataD3
20	I	N_SERTOCAM	Negative LVDS Input, Serial Communication to the camera
21	O	P_SERTOFG	Positive LVDS Output, Serial Communication from the camera
22	I	P_CC1	Positive LVDS Input, external Trigger signal EXSYNC
23	I	N_CC2	Negative LVDS Input, external clock for Slave mode MCLK
24	I	P_CC3	Positive LVDS Input, Exposure control EXPOSURE
25	I	N_CC4	Negative LVDS Input, Control signal CONTROL <not used>
26	PW	SHIELD	Shield
S	PW	SHIELD	Shield

**Table 4: Pin assignments for the socket of the voltage supply connector**

PIN	I/O	Name	Description
1	PW	VDD	+ 5 V voltage supply
2	PW	GND	Ground
3	PW	VDD2	Reserved



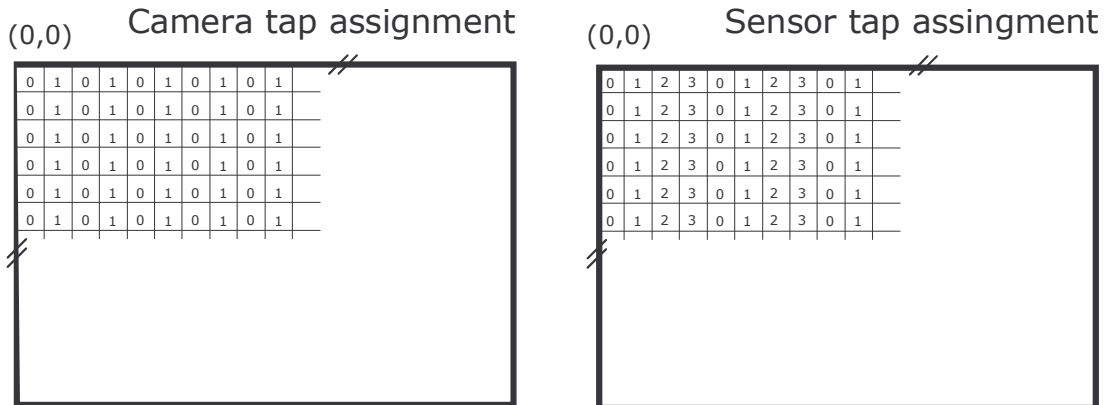
**Fig. 2: Connector socket Nr. 09-0408-90-03 for the voltage supply**

**Table 5: Data bit assignments for the 8 bit tap 0**

Data bit	CameraLink Port and bit
LSB	A0
LSB +1	A1
LSB +2	A2
LSB +3	A3
LSB +4	A4
LSB +5	A5
LSB +6	A6
MSB	A7

**Table 6: Data bit assignments for the 8 bit tap 1**

Data bit	CameraLink Port and bit
LSB	B0
LSB +1	B1
LSB +2	B2
LSB +3	B3
LSB +4	B4
LSB +5	B5
LSB +6	B6
LSB +7	B7


**Fig. 3: Camera and sensor pixel assignment**

### 3.2 LVDS Interface

To implement the LVDS (RS644) interface, the Molex 60 pole Low Force Helix (LFH60) plug system was used. This very compact plug system possess the property that the insertion force at the start of the insertion is very low and increases steadily as the plug is introduced. Due to the use of two contact points for each plug contact, the safety of the connection is substantially higher than that of other conventional systems. The Photonfocus LVDS Interface combines data and control signals as well as current supply on one socket. This has the advantage for the user that only one cable is needed between camera and frame grabber. **The contact pin sequence of the LFH60 system was altered from that used by the manufacturer (Molex).** Only the position of contact 1 is identical in the two systems. In contrast to the Molex system, in which the contacts are numbered in a meandering fashion, Photonfocus begins the count a new at the top of each column. The Photonfocus definitions are made clear in Table 7 and Fig. 4. Fig. 4 illustrate the pin assignments for the LVDS interface of the Photonfocus camera series. The interface definition contains the following: 16 data signals, 8 handshake signals for camera control by the frame grabber, an RS232 interface for camera set-up, as well as voltage supply. The 16 data signals can be used in different ways, depending on the camera type. The tap 0 uses the lower 8 bits (DATA0 ... DATA7). The tap 1 uses the upper 8 bits (DATA8 ... DATA15). The 8 handshake lines are divided between 4 input signals and 4 output signals. Input signals comprise the external trigger EXSYNC, the external exposure control EXPOSURE, the external clock signal for the slave mode (master clock) MCLK and an external camera control signal CONTROL. The camera output signals FRAME\_VALID, LINE\_VALID and PIXEL\_CLK are modeled on the AIA interface [AIA]. FRAME\_VALID high indicates an active image transfer. LINE\_VALID high denotes an active line. The digital data for the individual pixels are output on the rising edge of PIXEL\_CLK. In addition to these signals, the signal SHUTTER is defined to be high during the integration phase of the sensor. This signal permits the synchronization of external light sources e.g. a flash light (see section Timing Diagram).

**Table 7: LFH60 Socket pin assignment Molex Order number 70928-0002**

PIN	I/O	Name	Description
1	O	PDATA0	Positive LVDS Output, Data bit 0
2	O	PDATA2	Positive LVDS Output, Data bit 2
3	O	PDATA4	Positive LVDS Output, Data bit 4
4	O	PDATA6	Positive LVDS Output, Data bit 6
5	O	PDATA8	Positive LVDS Output, Data bit 8
6	O	PDATA10	Positive LVDS Output, Data bit 10, not used
7	O	PDATA12	Positive LVDS Output, Data bit 12, not used
8	O	PDATA14	Positive LVDS Output, Data bit 14, not used
9	O	PFRAME_VALID	Positive LVDS Output, FRAME_VALID
10	O	PLINE_VALID	Positive LVDS Output, LINE_VALID
11	I	PEXSYNC	Positive LVDS Input, external trigger signal EXSYNC
12	I	PEXPOSURE	Positive LVDS Input, external exposure control EXPOSURE
14	PW	GND	Ground
15	PW	GND	Ground
16	O	NDATA0	Negative LVDS Output, Data bit 0
17	O	NDATA2	Negative LVDS Output, Data bit 2
18	O	NDATA4	Negative LVDS Output, Data bit 4
19	O	NDATA6	Negative LVDS Output, Data bit 6
20	O	NDATA8	Negative LVDS Output, Data bit 8
21	O	NDATA10	Negative LVDS Output, Data bit 10, not used
22	O	NDATA12	Negative LVDS Output, Data bit 12, not used
23	O	NDATA14	Negative LVDS Output, Data bit 14, not used
24	O	NFRAME_VALID	Negative LVDS Output, FRAME_VALID
25	O	NLINE_VALID	Negative LVDS Output, LINE_VALID
26	I	NEXSYNC	Negative LVDS Input, external trigger signal EXSYNC
27	I	NEXPOSURE	Negative LVDS Input, external exposure control EXPOSURE
29	PW	GND	Ground
30	PW	GND	Ground
31	O	NDATA1	Negative LVDS Output, Data bit 1
32	O	NDATA3	Negative LVDS Output, Data bit 3
33	O	NDATA5	Negative LVDS Output, Data bit 5
34	O	NDATA7	Negative LVDS Output, Data bit 7
35	O	NDATA9	Negative LVDS Output, Data bit 9
36	O	NDATA11	Negative LVDS Output, Data bit 11, not used
37	O	NDATA13	Negative LVDS Output, Data bit 13, not used
38	O	NDATA15	Negative LVDS Output, Data bit 15, not used
39	O	NSHUTTER	Negative LVDS Output, active integration SHUTTER / FLASH
40	O	NPIXEL_CLK	Negative LVDS Output, PIXEL_CLOCK
41	I	NCONTROL	Negative LVDS Input, Control signal CONTROL <not used>
42	I	NMCLK	Negative LVDS Input, External clock for Slave mode MCLK
43	I	RX_RS232	RX, RS232 Camera Interface, RS232 Signal level
44	PW	VDD	+ 5 V Voltage supply
45	PW	VDD	+ 5 V Voltage supply
46	O	PDATA1	Positive LVDS Output, Data bit 1
47	O	PDATA3	Positive LVDS Output, Data bit 3
48	O	PDATA5	Positive LVDS Output, Data bit 5
49	O	PDATA7	Positive LVDS Output, Data bit 7
50	O	PDATA9	Positive LVDS Output, Data bit 9
51	O	PDATA11	Positive LVDS Output, Data bit 11, not used
52	O	PDATA13	Positive LVDS Output, Data bit 13, not used
53	O	PDATA15	Positive LVDS Output, Data bit 15, not used
54	O	PSHUTTER	Positive LVDS Output, active integration SHUTTER / FLASH
55	O	PIXEL_CLK	Positive LVDS Output, PIXEL_CLOCK
56	I	PCONTROL	Positive LVDS Input, Control signal CONTROL <not used>
57	I	PMCLK	Positive LVDS Input, External clock for Slave mode MCLK
58	O	TX_RS232	TX, RS232 Camera Interface, RS232 Signal level
59	PW	VDD	+ 5 V Voltage supply
60	PW	VDD	+ 5 V Voltage supply
S	PW	SHIELD	Shield
13, 28	PW	--	Reserved

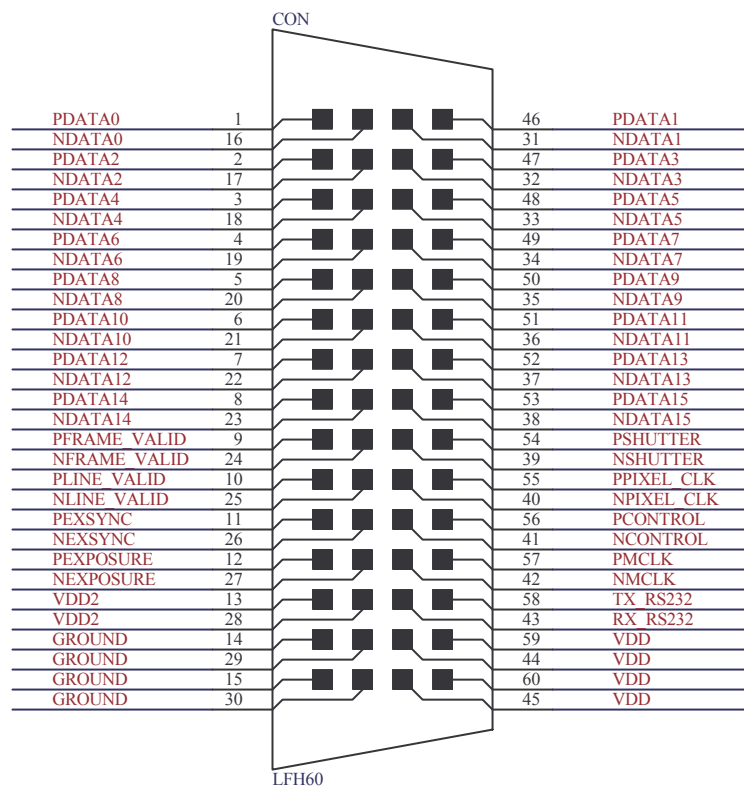
PW: Voltage supply

I: Input

O: Output

**Table 8: Contact pin sequence for the LFH60 plug system of the MV-D752 camera series**

Column	Pin numbers
1	Start at Molex mark 1 → 1 ... 15
2	Count continuation below Pin 1 16 ...30
3	Count continuation below Pin 16 31 ...45
4	Count continuation below Pin 31 46 ...60


**Fig. 4: View of LFH60 socket on rear of camera with signal allocations**

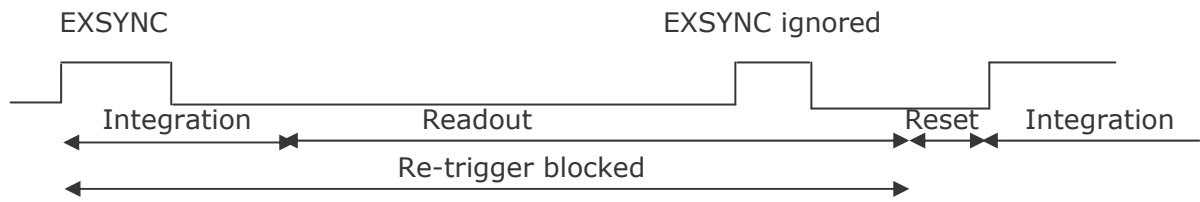
## 4 Status indicator

A two color LED on the rear of the camera indicates the camera status to the user. In normal operation the LED lights green when an image is being produced. At low frame rates a flickering can be observed that changes to a continuous light at high frame rates. Since the light intensity is dependent on the relation between exposure time and read-out time, the light from the LED can practically disappear when using small ROI and long exposure times.

A red LED indicates that serial communication is active.

## 5 Timing Diagrams

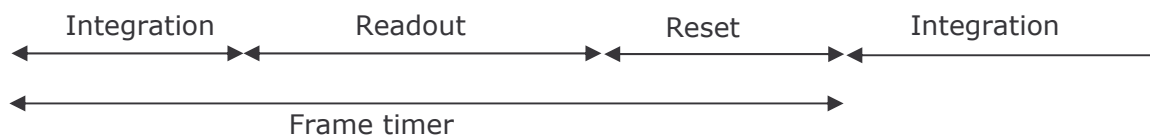
The parameter constant image data rate bit 1 register 12 has several functions. In free running mode it enables the acquisition of images with constant image data rate. If this parameter is deactivated, the data rate is determined directly by the exposure time and the readout time. In trigger mode, re-triggering during the frame time by an external trigger signal is suppressed. If deactivated, readout can be interrupted by a new trigger. In this mode the user should ensure that the trigger rate and the frame rate correspond. Fig. 5 illustrates the function of the parameter constant image data rate.



External trigger mode constant image data rate



External trigger mode variable image data rate



Free running mode constant image data rate



Free running mode variable image data rate

**Fig. 5: Function of the parameter constant image data rate**

### 5.1 Free running mode

The pre-installed free running mode allows images to be acquired without external control signals. The sensor will be read out after the set integration time; then the sensor will be reset. Following this, integration starts again and the readout of the image information begins afresh. The data are output on the rising edge of the pixel clock. The signals FRAME\_VALID (FVAL) and LINE\_VALID (LVAL) mask valid image information. The signal SHUTTER indicates the active integration phase of the sensor. The number of clock pulses after exposure **CPRE** is defined by the calculation of the frame time (see 5).

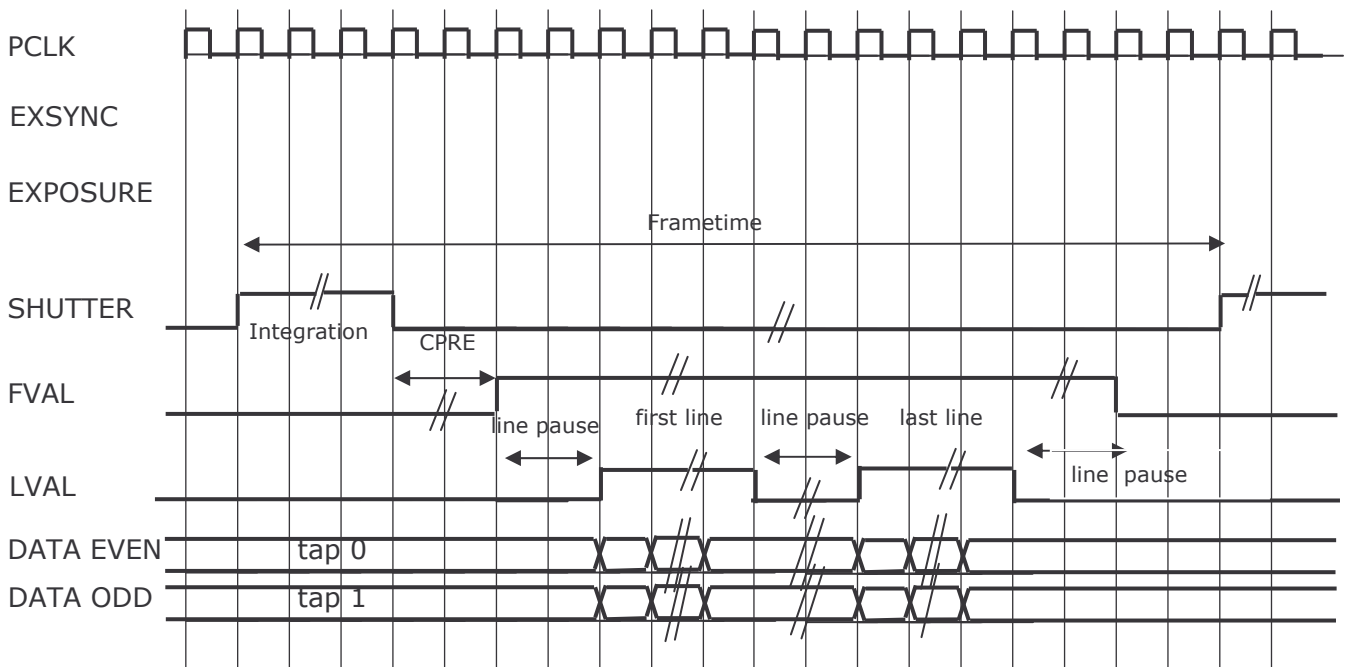


Fig. 6: Timing Diagram Free Running Mode

### 5.2 Trigger mode

In trigger mode image acquisition begins with the rising edge of an external trigger pulse (POLARITY\_SYNC\_EXPOSURE = '1'). The image will be read out after the preset exposure time. After readout, the sensor returns to the reset state and the camera waits for a new trigger pulse. If necessary, the polarity of the EXSYNC signal can be matched to that of the frame grabber by means of the flag POLARITY\_SYNC\_EXPOSURE bit 3 mode register 3.

The data are output on the rising edge of the pixel clock. The signals FRAME\_VALID (FVAL) and LINE\_VALID (LVAL) mask valid image information. The signal SHUTTER indicates the active integration phase of the sensor. The number of clock pulses after exposure CPRE is defined by the calculation of the frame time (see 5).

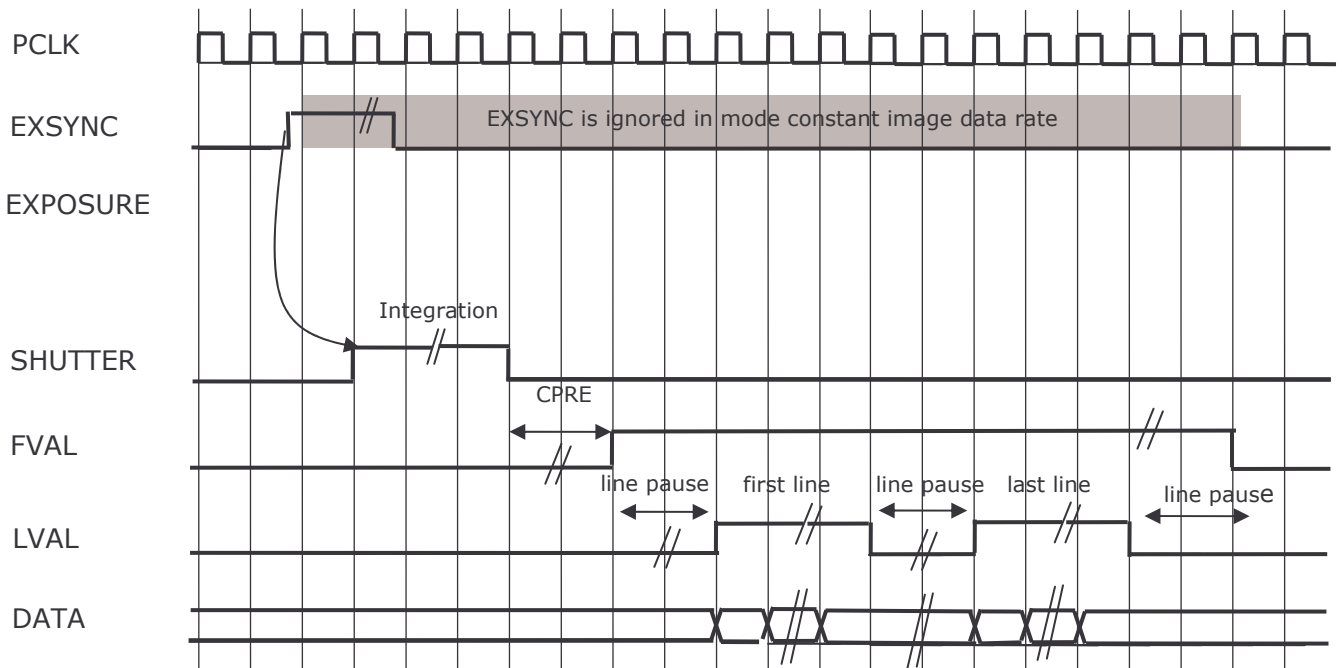


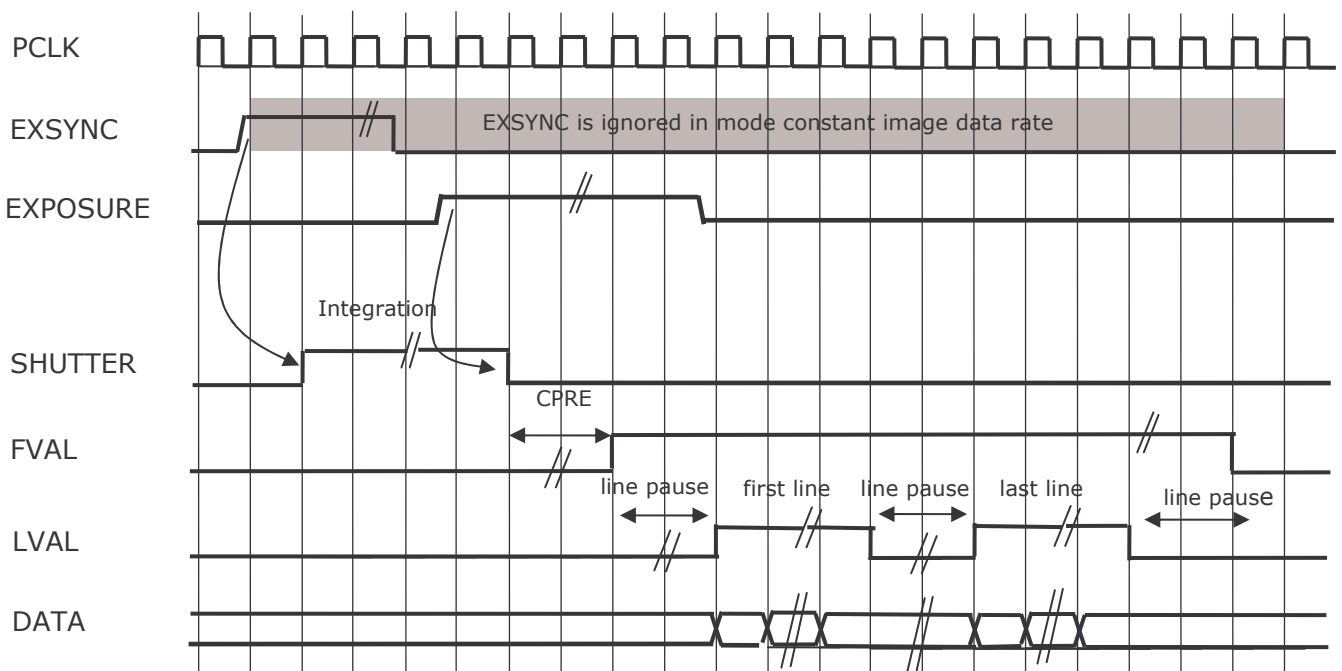
Fig. 7: Timing Diagram Trigger Mode

### 5.3 Trigger mode with external edge triggered exposure control

In trigger mode with external edge triggered exposure control, sensor control is reset with the rising edge of an external trigger pulse ( $POLARITY\_SYNC\_EXPOSURE = '1'$ ) and the exposure of the image begins. The integration ends with the rising edge of the external signal EXPOSURE ( $POLARITY\_SYNC\_EXPOSURE = '1'$ ). The signals EXSYNC and EXPOSURE are clocked in the sensor control in such a way that the internal exposure control becomes active one clock (50 ns in case of internal clock) later (see SHUTTER signal). If necessary, the polarity of the EXSYNC signal can be matched to that of the frame grabber by means of the flag  $POLARITY\_SYNC\_EXPOSURE$  bit 3 mode register 3.

The image is read out after the exposure time has elapsed. After readout, the sensor returns to the reset state and the camera waits for a new trigger pulse.

The data are output on the rising edge of the pixel clock. The signals FRAME\_VALID (FVAL) and LINE\_VALID (LVAL) mask valid image information. The signal SHUTTER indicates the active integration phase of the sensor. The number of clock pulses after exposure **CPRE** is defined by the calculation of the frame time (see 5).



**Fig. 8: Timing Diagram Trigger Mode with external edge triggered exposure control**

### 5.4 Sync-exposure mode

In Sync-Exposure mode, sensor control is reset with the rising edge of an external trigger pulse EXSYNC and the exposure of the image begins. The integration ends with the falling edge of the external signal EXSYNC. The signal EXSYNC is clocked in the sensor control in such a way that the internal exposure control becomes active one clock (35 ns in case of internal clock) later (see SHUTTER signal). If necessary, the polarity of the EXSYNC signal can be matched to that of the frame grabber by means of the flag POLARITY\_SYNC\_EXPOSURE bit 3 mode register 3.

The image is read out after the exposure time has elapsed. After readout, the sensor returns to the reset state and the camera waits for a new trigger pulse.

The data are output on the rising edge of the pixel clock. The signals FRAME\_VALID (FVAL) and LINE\_VALID (LVAL) mask valid image information. The signal SHUTTER indicates the active integration phase of the sensor. The number of clock pulses after exposure CPRE is defined by the calculation of the frame time (see 5).

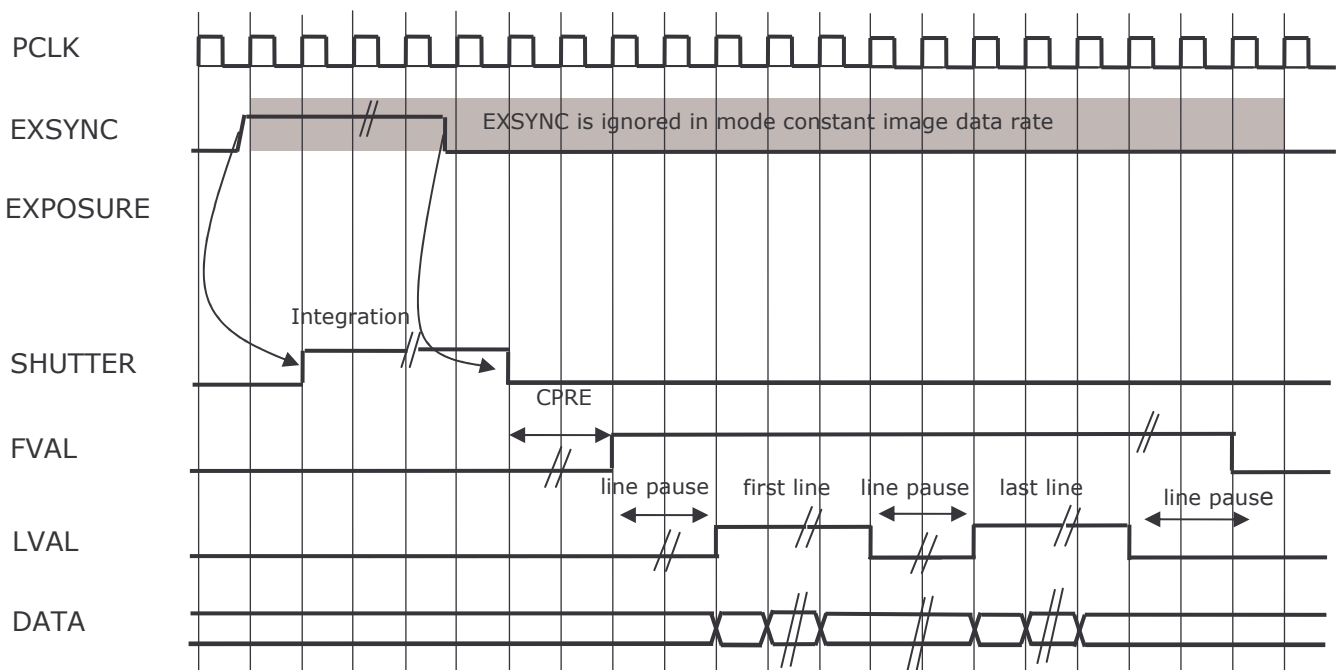


Fig. 9: Timing Diagram Sync-Exposure Mode

## 5.5 Overview of the trigger modes

The following overview summarizes the functions of the various trigger modes.

Polarity	TRIGGER START	EXPOSURE START	EXPOSURE STOP
EXSYNC Mode internal exposure time via Register			
- 1	FE_EXSYNC	FE_EXSYNC	EXPOSURE_END
+1	RE_EXSYNC	RE_EXSYNC	EXPOSURE_END
EXSYNC - EXPOSURE Start/Stop Trigger for exposure time			
- 1	FE_EXSYNC	FE_EXSYNC	FE_EXPOSURE
+1	RE_EXSYNC	RE_EXSYNC	RE_EXPOSURE
EXSYNC-EXPOSURE			
- 1	FE_EXSYNC	FE_EXSYNC	RE_EXSYNC
+1	RE_EXSYNC	RE_EXSYNC	FE_EXSYNC

RE\_xxxx: Rising Edge of signal  
 FE\_xxxx: Falling Edge of signal

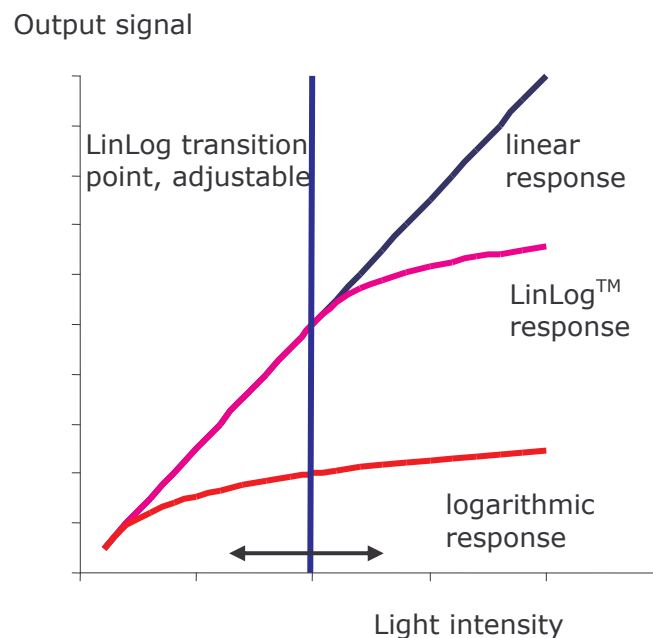
## 6 Variation of the sensor characteristics

The LinLog™ CMOS image sensors from Photonfocus afford the user the possibility to adapt the characteristics of the sensor to the requirements of the application.

For normal applications that do not require high contrast, the sensor can be operated in linear mode. For applications having short exposure times and low illumination intensity, it is advisable to activate skim mode, in which a non-linear amplification, similar to a gamma correction, occurs in the pixel so that small signals are amplified significantly more than large signals (see Variation of the amplification).

In situations involving high intrascene contrast, compression of the upper gray level region can be achieved with the LinLog™ Technology. At low intensities, each pixel shows a linear response. At high intensities, the response changes to logarithmic compression. The transition region between linear and logarithmic response can be smoothly adjusted and is continuously differentiable. This setting is achieved via DAC channel 4 in the voltage range 0 – 4V (see Appendix E).

For many applications the logarithmic compression of the LinLog™ mode is too large. For this reason the LinLog2™ technique was developed by Photonfocus to allow a significantly more moderate transition between the two response regions. In addition, two further parameters (lower LinLog value and LinLog2 time) were introduced to control the transition. At the beginning of the exposure time, high intensities are integrated with the upper LinLog value, i.e. strong logarithmic compression. After time LinLog2, the lower LinLog value is activated and lower intensities are integrated with almost linear response. By varying these three parameters the response can be adjusted to the needs of the application over a wide range. A detailed description of the LinLog2™ technique is explained in Photonfocus Application note [AS001].

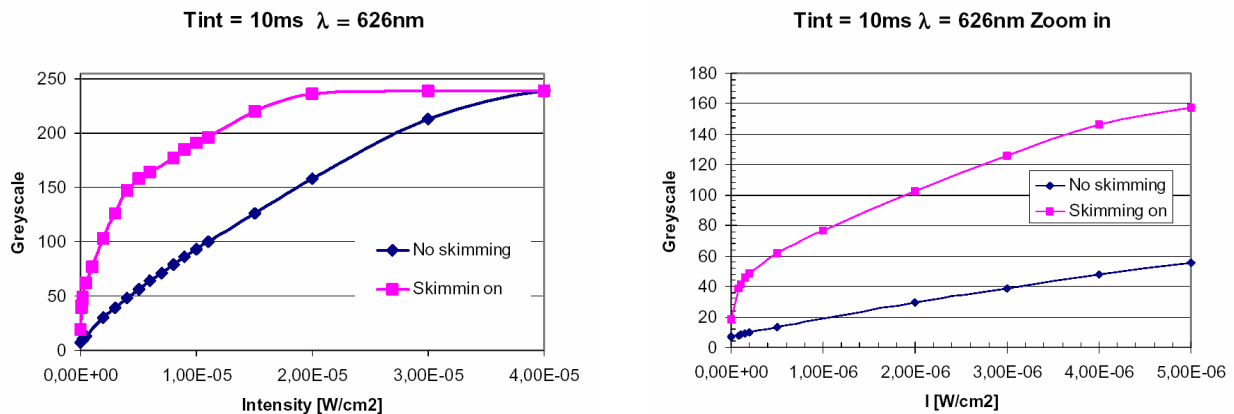


**Fig. 10: Response of the various camera modes**

## 7 Variation of the amplification

The MV-D752-80 camera contains several possibilities for amplifying the video signal. On the one hand the CMOS sensor can be operated in skim mode, corresponding to a non-linear amplification. In this mode low intensities are amplified more strongly than high intensities (small signal amplification). The resulting response is similar to a gamma correction. Fig. 11 shows an example of sensor response for a fixed skim voltage in comparison with the linear response of the sensor. The right hand figure represents a zoom of the lower intensity region. The small signal amplification is the relation between the sensor output voltages of both modes at constant low illumination. The skim voltage can be varied via DAC channel 3 in the voltage range 0 – 4V (see Appendix E). An unsuitable choice of parameters can lead to image lag with high contrast scenes, resulting in smearing of the image and reduced image quality. A skim voltage of 1.4V, corresponding to a small signal amplification of about 2, turns out to be a reasonable value in practice.

In Skim mode, please note: **Exposure time <10ms; LinLog voltage < 1V. To increase the shutter efficiency a LinLog value of 25 should be used!** Furthermore, when using this mode constant frame time the frame time should be set to a value that allows the sensor a reset time of at least 10  $\mu$ s.



**Fig. 11: Sensor response in Skim mode compared with linear response**

On the other hand, it is possible to switch the amplification of the video amplifier of the sensor module between amplification factors 1 and 4 by activating bit 7 register 7. The offset correction for the amplifier must then be adjusted. If option EN\_TOGGLE bit 4 register 6 is activated, the switch occurs automatically. In this case switching occurs between two preset offset values. If the automatic offset correction is deactivated, the user is responsible for suitably adjusting the correction. This is achieved for every operating mode by adjusting the video signal offset via DAC channel 5 (see Appendix E).

It is important to note that, when using these LUTs with a maximum gray level value of 255, the LinLog™ modes perform a compression of the upper gray level values and the contrast improvement cannot be attained with the pre-programmed LUTs. By suitably adjusting the LUTs, non-linear responses can be realized, allowing the gray level range of interest to be spread to suit the application. Moreover, response ranges of the LinLog™ modes can also be transferred to the 8-bit output resolution.

## 8 Change of resolution

With the MV-D752-80 CMOS camera, it is possible to increase the image data rate by reading out a part of the pixel matrix. The user can define a Region Of Interest (ROI) within the sensor to be transmitted to the frame grabber. The only restriction is that 64 pixels must be activated on both halves of the sensor in the x-direction. Having satisfied this condition, the readout speed of the sensor increases linearly with the decrease in the number of pixels in a row. In the y-direction any non-zero number of lines may be chosen. The image data rate increases linearly with the decrease in the number of readout lines. The smallest ROI for the camera thus consists of one line of 128 pixels, symmetrically arranged about the middle of the image. Table 9 gives an overview of the increase in image data rate with decrease in size of the ROI. Fig. 11 shows examples of various readout regions. The ROI is defined via registers 24 to 31.

If one requires total freedom in the choice of the ROI, the restriction described above can be removed by deactivating the pre-load of line addresses. This is achieved by deactivating bit 5 of mode register 3 (address 0DH), i.e. set EN\_PRELOAD = 0, and also setting the line pause register address 20H to a safe value greater than 32.

Another possible way to increase the image data rate is to jump over lines (Line Hopping). In this mode the camera delivers a pseudo-image to the frame grabber consisting of the composition of individual selected lines. The MV-D752-80 camera allows the user to define the jump distance via the 8-bit parameter Line jump (register 33, see sensor module register description), whose value can be in the range 1 to 255. This mode is activated by bit 4 register 12. Line hopping can also be used in a pre-defined ROI.

The two modes Row hopping and Decimation are in preparation.

**Table 9: Maximum image data rates as a function of the resolution**

ROI Dimensions	Image data rate @ 20 MHz clock rate, $T_{int} = 10 \mu s$
752 x 582	170 fps*
512 x 512	290 fps
256 x 256	1 100 fps
128 x 128	4 100 fps
128 x 16	24 000 fps
752 x 1	46 000 fps*

### 8.1 Flip Image

In the Flip Image mode, the readout direction of the sensor can be inverted so that the image appears upside down. This mode is activated by bit 2 register 12.

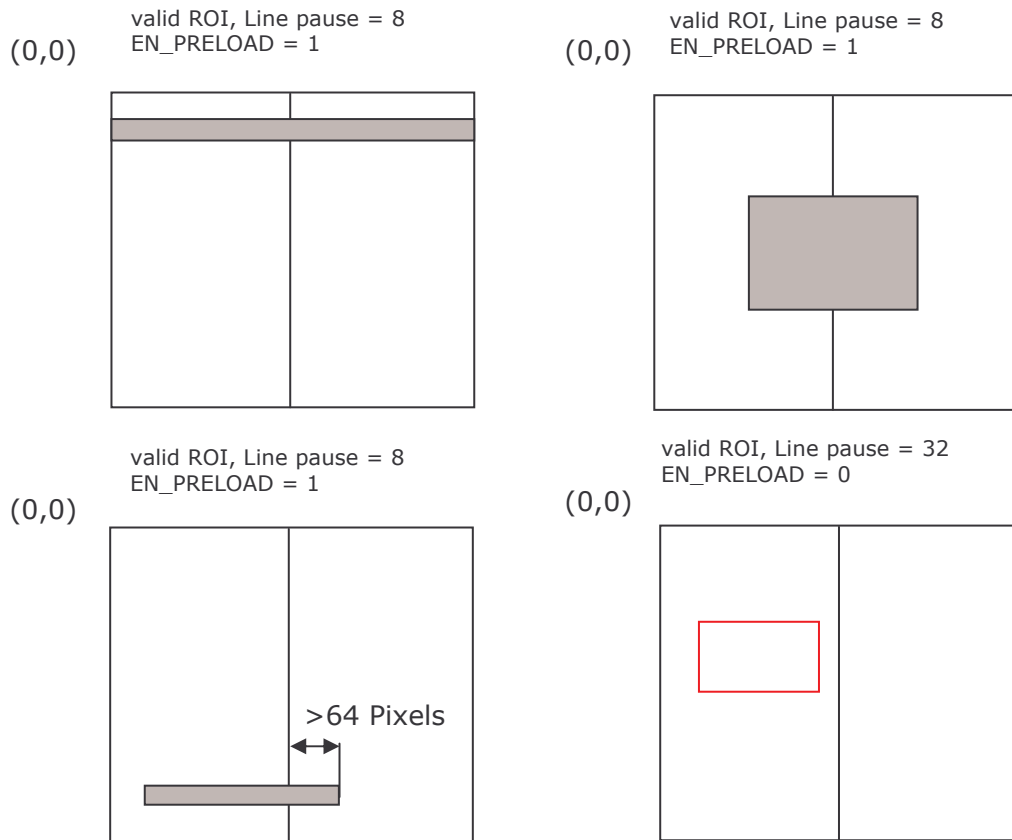


Fig. 12: Examples of ROIs with line address pre-load

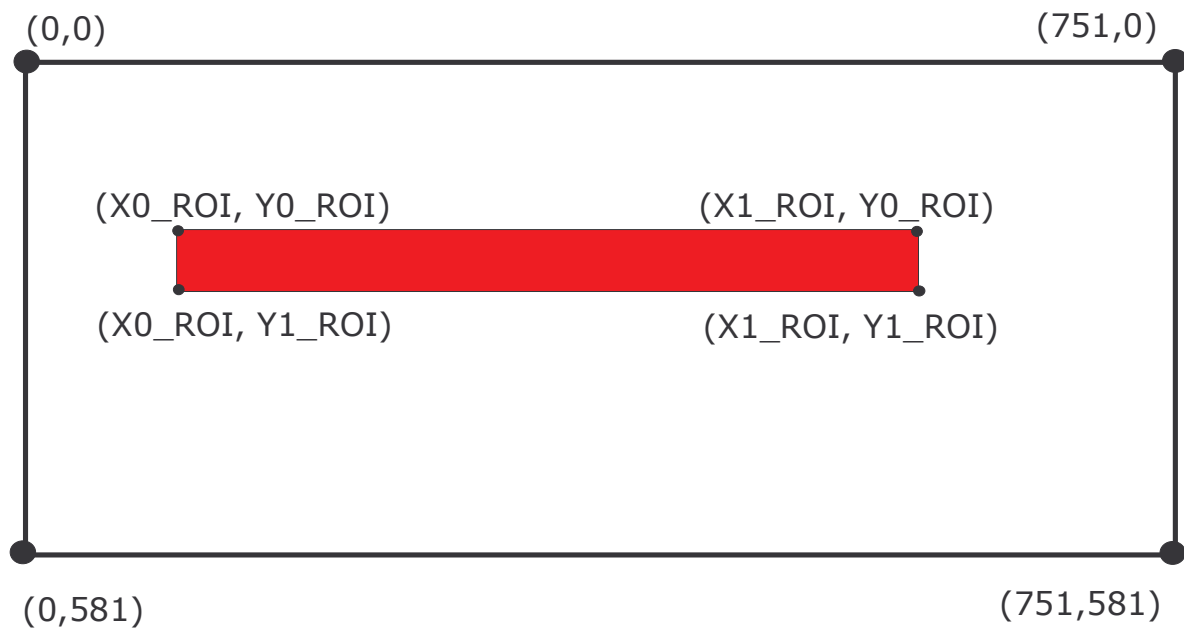


Fig. 13: A single ROI bounded by  $(X0\_ROI, Y0\_ROI)$  and  $(X1\_ROI, Y1\_ROI)$

## 8.2 Correction of manufacturing allowances

For fine corrections of the image window, offset parameters in X and Y directions are needed. With the X\_OFF and Y\_OFF parameters, the manufacturing tolerances of the centering of the optical axis on the sensor can be corrected. For ideal centering of the optical axis of the camera on the sensor, the following values of X\_OFF and Y\_OFF are used.

$$X\_OFF = \frac{1}{2} (1024 - 752) = 136 \rightarrow 88H$$

$$Y\_OFF = \frac{1}{2} (1024 - 582) = 221 \rightarrow DDH$$

Based on these ideal values, the real values are adjusted upon factory delivery. X\_OFF and Y\_OFF are stored in Registers 34 and 36. The maximum value of X\_OFF and Y\_OFF are X\_OFFmax = 255 und Y\_OFFmax = 255.

## 9 Camera function test

An Linear Feedback Shift Register (LFSR), activated by flags ENABLE2 = 1 and ENABLE3 = 1 (bits 2 und 3) register 6, was implemented to test the camera interface to the frame grabber. Appendix F contains a detailed description of the LFSR.

## 10 Description of the camera sensor registers

The operating modes and functions of the camera are defined and set by internal registers. The internal camera registers are initialized at camera boot up, which occurs either when the camera is switched on or following a camera reset from the software interface. The contents of the camera registers are copied into the registers from a non-volatile re-write able memory (Boot-EEPROM). After camera boot up, the camera is fully operational and the operating modes and functions correspond to the loaded initial values.

Factory settings are free-running mode, 8-bit resolution and linear response. An example of initial sensor control values is summarized in Table 28. Since every camera is individually set up before delivery, parameters will vary from those shown in Table 28. **For that reason the user should back up the factory settings of the new camera to a storage medium at the beginning of the hardware installation. This enables the restoration of factory settings by the user in the event of incorrect programming or storing of camera parameters by the user. Programs and software routines supplied by Photonfocus AG should be used for backup and restoration of the factory settings!**

The basic settings of the camera can be changed by the user and stored in the Boot-EEPROM. It is advisable, in the first instance, to set the camera functions or parameters via the software interface and to test them in the application. Once the parameters have been successfully tested, they can be stored as user settings. Photonfocus AG provides programs and software routines for this purpose [SOFT], [PFREMOTE]. **Low level programming of the module hardware independently of the API function library will not be supported by Photonfocus!** It is advisable to back up the user settings in the same manner as that for the factory settings.

The internal modules for camera configuration work independently of the modules for image acquisition. For ROI and exposure time, both modules are separated by shadow registers, which are updated at the end of the image (falling edge of FRAME\_VALID).

**10.1 Register assignment - sensor control group**
**Table 10: Sensor control registers, address 0 to 31**

REG DEC	REG HEX	R/W or B	description
0	0	R/W	Data EEPROM
1	1	W	LSB address EEPROM/Status register 0 =>46H = "F" hard coded
2	2	W	MSB address and OP-Code EEPROM/Status register 1 => HW revision hard coded
3	3	C	Command SEND_PROM, content of registers 0 – 2 are sent to the EEPROM
4	4	C/R	Command RELOAD of the registers / Status register has 3 internal states
5	5	R/W	Status register 4 internal states
6	6	R/W	Mode register 0 , adjust camera modes
7	7	R/W	Mode register 1 , adjust camera modes
8	8	W	LSB DAC, see Appendix E
9	9	W	MSB DAC, see Appendix E
10	A	-	Not used
11	B	-	Not used
12	C	R/W	Mode register 2 , adjust camera modes
13	D	R/W	Mode register 3 , adjust camera modes
14	E	R/W	Mode register 4 , adjust camera modes
15	F	R/W	LSB Exposure Time
16	10	R/W	MSB-1 Exposure Time
17	11	R/W	MSB Exposure Time
18	12	R/W	LSB LinLog Time
19	13	R/W	MSB-1 LinLog Time
20	14	R/W	MSB LinLog Time
21	15	R/W	LSB Frame pause
22	16	R/W	MSB-1 Frame pause
23	17	R/W	MSB Frame pause
24	18	R/W	LSB ROI-X0 boundary condition for Region Of Interest (ROI) Sensor matrix
25	19	R/W	MSB ROI-X0 boundary condition for Region Of Interest (ROI) Sensor matrix (*)
26	1A	R/W	LSB ROI-Y0 boundary condition for Region Of Interest (ROI) Sensor matrix
27	1B	R/W	MSB ROI-Y0 boundary condition for Region Of Interest (ROI) Sensor matrix (*)
28	1C	R/W	LSB ROI-X1 boundary condition for Region Of Interest (ROI) Sensor matrix
29	1D	R/W	MSB ROI-X1 boundary condition for Region Of Interest (ROI) Sensor matrix (*)
30	1E	R/W	LSB ROI-Y1 boundary condition for Region Of Interest (ROI) Sensor matrix
31	1F	R/W	MSB ROI-Y1 boundary condition for Region Of Interest (ROI) Sensor matrix (*)

Abbreviations:

R: Read  
W: Write  
C: Command  
DEC: decimal value  
HEX: hexadecimal value  
(\*): bit 2 to 7 arbitrary value

**Continuation Table 10: Sensor control registers, address 32 to 63**

REG DEC	REG HEX	R/W or B	Description
32	20	R/W	Line pause
33	21	R/W	Interlacing
34	22	R/W	Offset parameter in x direction
35	23	-	Not used, reserved for MSB offset parameter in x direction
36	24	R/W	Offset parameter in y direction
37	25	-	Not used, reserved for MSB offset parameter in y direction
38	26	-	Not used
39	27	-	Not used
40	28	-	Not used
41	29	-	Not used
42	2A	-	Not used
43	2B	-	Not used
44	2C	-	Not used
45	2D	-	Not used
46	2E	-	Not used
47	2F	R/W	Choice of a RAM bank for read-/write access
48	30	R/W	Byte0 of a 16x8 RAM-Bank
49	31	R/W	Byte1 of a 16x8 RAM-Bank
50	32	R/W	Byte2 of a 16x8 RAM-Bank
51	33	R/W	Byte3 of a 16x8 RAM-Bank
52	34	R/W	Byte4 of a 16x8 RAM-Bank
53	35	R/W	Byte5 of a 16x8 RAM-Bank
54	36	R/W	Byte6 of a 16x8 RAM-Bank
55	37	R/W	Byte7 of a 16x8 RAM-Bank
56	38	R/W	Byte8 of a 16x8 RAM-Bank
57	39	R/W	Byte9 of a 16x8 RAM-Bank
58	3A	R/W	Byte10 of a 16x8 RAM-Bank
59	3B	R/W	Byte11 of a 16x8 RAM-Bank
60	3C	R/W	Byte12 of a 16x8 RAM-Bank
61	3D	R/W	Byte13 of a 16x8 RAM-Bank
62	3E	R/W	Byte14 of a 16x8 RAM-Bank
63	3F	R/W	Byte15 of a 16x8 RAM-Bank

**Abbreviations:**

R: Read  
 W: Write  
 C: Command  
 DEC: decimal value  
 HEX: hexadecimal value

**10.2 Register description - sensor control group**
**10.2.1 Register address 00H – 03H (EEPROM control)**

The first 4 registers are used to communicate with the EEPROM of the camera. The read/write register address 00H contains the data for the EEPROM. The register addresses 01H and 02H are write-only and contain the EEPROM R/W addresses as well as the OP-code. Register address 03H is used as a command for accessing the EEPROM. More information can be found in Appendix D.

**10.2.2 Register Addresses 1, 2, 4 and 5: status registers 0, 1, 3 and 4**

Status register 0 (address 01H) contains the **signature byte 46H = ASCII F**. Status register 1 (address 02H) contains the hardware revision. The bits of status register 3 (address 04H) and status register 4 (address 05H) are used for internal states of the sensor control group. Sensor module status information is available in status register 3, while intermittent errors occurring during the operation of the camera are stored in status register 4. The error bits in status register 4 can be reset by writing a logical '1' to the corresponding bit.

The definitions of the individual bits of these registers are summarized in Table 11 and Table 12. Bit 0 and bit 1 of status register 3 contain information about the state of the EEPROM when storing camera settings. If the camera is in the AUTOLOAD state (after power-on or reset of the camera), the settings are being copied from the EEPROM to the internal registers. **During this phase, EEPROM access is not permitted because otherwise incorrect information will get into the internal camera register.** The PROM\_BUSY state indicates an uncompleted writing cycle (active memory load) during write access to the EEPROM. **EEPROM access in this condition should always be avoided!** Bit 2 serves as a signature bit for the sensor module and is permanently set to zero.

**Table 11: Status register 3 (register address REGADDR = 4D = 04H)**

Register address 4 - STATUS3_REG		
bit	Description	Default
0	= 1 → AUTOLOAD, signals power-up or Reload of data (from EEPROM), <b>! No write operations to EEPROM allowed !</b>	0
1	= 1 → PROM_BUSY, <b>! No write operations to EEPROM allowed !</b>	0
2	always 0 → sensor module	0
3	Not used = 0	0
4	Not used = 0	0
5	Not used = 0	0
6	Not used = 0	0
7	Not used = 0	0

Bit 0 of status register 4 indicates a transmission error during RS232 communication. This flag can be used to catch errors during read operations. Bit 1 of status register 4 indicates access to an undefined register. With read operations producing the result 18H = CANCEL, this bit can be used to distinguish between correct responses of the camera interface and an undefined state.

**Table 12: Status register 4 (register address REGADDR = 5D = 05H)**

Register address 5 - STATUS4_REG		
bit	Description	Default
0	Error in the RS232 transfer	0
1	CANCEL was active, i.e. read from not defined register	0
2	Not used = 0	0
3	Not used = 0	0
4	Not used = 0	0
5	Not used = 0	0
6	Not used = 0	0
7	Not used = 0	0

### 10.2.3 Register Addresses 6 and 7: Mode registers 0 and 1

The basic functions of the camera are controlled by mode registers 0 and 1. To ensure proper operation, these registers are updated first during power-up. The functions of each individual bit are shown in Table 13.

**Table 13: Mode register 0 (register address REGADDR = 6D = 06H)**

Register address 6 - MODE0_REG			
bit	Name	Description	Default
0	ENABLE0	Camera on, = 1 → Camera in operation	1
1	ENABLE1	Invert Pixel Clock, = 1 → phase shift of 180 degrees	0
2	ENABLE2	These bits are responsible for resolution, access to the LUT's and the LFSR interface test	0
3	ENABLE3		0
4	EN_TOGGLE	= 1 → automatic voltage switching active	1
5	EN_LL2_LOG	= 1 → LinLog2-response curve active	0
6	LOG	= 1 → Log-response curve on = 0 → Log-response curve off	0
7	LINLOG	= 1 → LinLog-response curve on = 0 → LinLog- response curve off	0

If the camera is deactivated by bit 0 register 6, then, for cameras with a CameraLink interface, the internal ADC as well as internal and external triggers are deactivated. For cameras with an LVDS interface, the LVDS drivers are additionally switched into the tri-state mode and bit 1 register 6 allows the phase of the PIXEL\_CLK to be matched to that of the frame grabber. **For cameras with a CameraLink interface, bit 1 must always be deactivated.**

Bits 2 and 3 switch the camera resolution. The function is described in Table 14. To test the camera interface and connection to the frame grabber, a pseudo-random number generator with a 8 bit Linear Feedback Shift Register (LFSR) was implemented. The pseudo-random number generator is reset at the beginning of each line so that conclusions can be drawn about the reliability of the interface by directly comparing the data received. The LFSR is described in Appendix F.

Bit 4 activates the automatic switching of factory set camera settings for pre-defined LinLog values and Skim values. It controls automatic offset compensation when switching to a high gain (bit 7 register 7) and the activation of the classical logarithmic mode (bit 6 register 6). In Skim mode, an active flag EN\_TOGGLE results in automatic switching to a factory set skim voltage (bits 5/6 register 7). Bit 5 activates the LinLog2 behavior.

Bit 6 register 6 switches the camera to logarithmic mode (classical logarithmic pixel in non-integrating mode). In this mode, **which is not supported by Photonfocus**, a gain of 4 should be activated, followed by an offset adjustment of the camera. The increased Fixed Pattern Noise (FPN ~50%) can be removed very effectively by a digital pixel-by-pixel offset correction (difference image technique, with a dark image as reference). Bits 5 and 7 should not be set in this mode.

Bit 7 register 6 activates the LinLog mode. It is used by the internal state machines to generate the LinLog characteristic. Consequently, this value toggles between 0 and 1 when the LinLog2 characteristic (EN\_LL2\_LOG = 1) is active.

**Table 14: Camera resolution and special functions**

Enable3	Enable2	Function	Description
0	0	8 bit	Digital gain x 1
0	1	8 bit	Digital gain x 2
1	0	8 bit LUT 9-to-8	four user programmable LUT's LUT0 factory preset LUT1 factory preset LUT2 factory preset LUT3 factory preset (See Appendix B)
1	1	8 bit LFSR	Interface test with Linear Feedback Shift Register (LFSR)

**Table 15: Mode register 1 (Register address REGADDR = 7D = 07H)**

Register address 7 - MODE1_REG			
bit	Name	Description	Default
0	HIGH_VB1	= 1 → increase current in source VB1	0
1	HIGH_VB2	= 1 → increase current in source VB2	0
2	HIGH_VB3	= 1 → increase current in source VB3	0
3	CURR_ON	= 1 → current sources on, = 0 → Current sources off	0
4	EN_DUMMY	= 1 → Dummy line on = 0 → Dummy line off	0
5	SKIM_IMAGE0	= 1 → Skim voltage 0 on, = 0 → Skim voltage 0 off	0
6	SKIM_IMAGE1	= 1 → Skim voltage 1 on, = 0 → Skim voltage 1 off	0
7	HIGH_GAIN	= 1 → Gain by 4, = 0 → gain by 1	0

Before you modify mode register 1 (bits 0 to 3), please contact Photonfocus Ltd. because of a possible malfunction or limited function of the sensor after modifying these values. With the help of the dummy line, the transfer of data from the sensor to the frame grabber card can be easily tested.

When the bits 5 to 7 are switched on (or off), a possible bias re-tuning of the video amplifier is required.

#### **10.2.4 Register Addresses 8 and 9: DAC interface**

The registers 08H and 09H are used for the DAC access and for adjustments to the camera in the various operating modes. To access the DAC, please refer to Appendix E. Please do not modify these values unless you really need to change some specific values.

**A wrong value can cause a malfunction of the camera!**

The DAC has 8 channels (Channels 0 – 7), corresponding to the functions listed in Table 16. To avoid malfunctioning of the camera, voltages outside the stated ranges should not be used.

**Table 16: Assignments of the DAC channels**

Channel	Name	Description	Voltage range/V
0	VB1	External force VB1, pixel bias	0.6 – 0.8
1	VB2	External force VB2, column bias	2.0 – 2.4
2	VB3	External force VB3, output bias	0.7 – 0.9
3	VSH	Shutter voltage	0.0 – 4.0
4	VLOG	LinLog voltage	0.0 – 4.0
5	Global_offset	Offset voltage for video output amplifier	1.3 – 1.5 Low Gain 2.0 – 2.2 High Gain
6	Video_black	Not used at the moment	-
7	Sync_offset	Not used at the moment	-

#### **10.2.5 Register Addresses 12-14: Mode register extended functions**

The registers 12 – 14 contains further bits for camera adjustment. Register 12 contains further basic settings for the camera. Register 13 contains the control bits for the extended trigger modes and functions to deactivate the pre-load of the sensor column addresses. Register 14 contains the flag for switching communication to the ADC module.

**Table 17: Mode register 2 (register address REGADDR = 12D = 0CH)**

Register address 12 - MODE2_REG			
bit	Name	Description	Default
0	SYNC_EXTERN	= 1 → external synchronization	0
1	CONST_FRAMERATE	= 1 → constant frame rate	1
2	FLIP_IMAGE	= 1 → output picture upside-down	0
3	Not used	-	0
4	EN_LINE_HOPPING	= 1 → switch on line hopping	0
5	Not used	-	0
6	EN_GLOBAL_RESET	= 1 → switch on global reset of the sensors	1
7	EN_MCLK	= 1 → activate external pixel clock	0

Several cameras can be exactly synchronized (assuming equal cable lengths) by activating the external clock. As an example, this could be used in stereo vision applications.

**Table 18: Mode register 3 (Register address REGADDR = 13D = 0DH)**

Register address 13 - MODE3_REG			
bit	Name	Description	Default
0	Not used	-	0
1	EN_EXPOSURE_FT	External shutter control by edge triggering EXSYNC and EXPOSURE, shutter opens on positive edge of EXSYNC signal, shutter closes on positive edge of EXPOSURE signal	0
2	EN_SYNC_EXPOSURE	External triggering and shutter control by EXPOSURE signal, shutter opens on positive edge of EXPOSURE signal and EXSYNC is on, shutter closes on negative edge of EXPOSURE Signal	0
3	POLARITY_SYNC_EXPOSURE	= 1 → SYNC_EXPOSURE active HIGH, i.e. rising edge EXSYNC signal = EXSYNC and EXPOSURE on, falling edge EXSYNC Signal = EXPOSURE off	1
4	EN_SHUTTER	= 1 → SHUTTER Signal active, <b>for CameraLink standard set 0 → DVAL = 1</b>	0
5	EN_PRELOAD	= 1 → enable line preload	1
6	EN_LINE_RESET	= 1 → enable line reset at in the middle of a line	0
7	EN_HOLD_READOUT	= 1 → enable HOLD function, in development	0

**Table 19: Mode register 4 (register address REGADDR = 14D = 0EH)**

Register address 14 - MODE4_REG			
bit	Name	Description	Default
0	SLAVE_ACTIVE	= 1 → enable RS232 interface ADC module	0
1	Not used	-	0
2	Not used	-	0
3	Not used	-	0
4	Not used	-	0
5	Not used	-	0
6	Not used	-	0
7	Not used	-	0

Bits 0 to 3 mode register 3 determine the trigger modes in Slave mode. These trigger modes can only be activated in the external trigger mode bit 0 = 1 mode register 2. The user can, however, only select one of the two special trigger functions in the camera. If the slave modes are not activated and the camera is externally synchronized, then the exposure time is determined by the value Exposuretime Register 15 – 17.

Bit 4 activates the signal SHUTTER. With the CameraLink interface, this bit is deactivated so that DVAL = 1, corresponding to the CameraLink standard.

Bit 5 activates the preload of the line addresses, minimizing the line delay and allowing very high frame rates to be achieved. The pre-load of the line addresses in the middle of the line limits the free choice of ROI. To circumvent this limitation, the pre-load should be deactivated and the line delay register 32 increased to a value greater than 32.

Bit 6 activates the half-line reset. When used with Skim mode, the sensor can be put into an extended rest phase resulting, with certain settings, in the production of image artifacts. Photonfocus recommends that this bit be deactivated.

Bit 7 activates the HOLD\_READOUT mode, which allows transmission to be interrupted when the CONTROL signal is active. The 'hold' occurs after the end of a line.

### **10.2.6 Registers 15-17: Exposure time**

The exposure time (parameter Exposuretime) is implemented in a 24 bit register. This register consist of three 8 bit registers register 15-17. This value is also set in increments of the pixel clock (50 ns in case of the internal camera clock). The exposure time can be varied during read out of the sensor, because actual value is stored in a shadow register.

### **10.2.7 Registers 18-20: for LinLog2**

The LinLog2 time constant is also implemented as a 24 bit register (registers 18-20), just as the exposure time. The LinLog2 time constant must always be smaller than the exposure time.

### **10.2.8 Registers 21-23: Frame time**

The frame pause is set by register 21-23. This value is also set in increments of the pixel clock (50 ns in case of the internal camera clock) as both of the above time values. The frame pause is used to keep the frame rate constant, independent of the exposure time. **NOTICE:** the frame rate sets the maximum exposure time. Invalid values must be prevented via software.

### **10.2.9 Registers 24-31: ROI**

The registers 24-31 are used to define the region of interest of the sensor (see Fig.12). The coordinates of the corners of the ROI can be written at every time into the shadow registers. After read out of a frame the values of the shadow registers are mirrored into the working registers. Invalid values must be prevented via software. Values  $x_0 > x_1$  or  $y_0 > y_1$  are ignored by the camera. In this cases the coordinates of the corners of the ROI are  $x_0 = 0$  and  $x_1 = 751$  or  $y_0 = 0$  and  $y_1 = 581$ . **When changing the ROI, note that some frame grabbers expect defined line and row settings and these values must be updated in the corresponding files.**

### **10.2.10 Register 32: Line pause**

This register holds the line pause value, in units of the pixel clock ( $t_u = 50\text{ns}$ ). The range of values is 8 .. 255. If the pre-load of line addresses is deactivated, then the minimum line pause of 8 cannot be reached! **When changing the line pause, note that some frame grabbers expect defined line pause settings and these values must be updated in the corresponding files.**

### 10.2.11 Calculation of Frame time

The frame rate depends on the parameters exposure time, frame pause, ROI and line pause. For the frame rate:

$$\text{Frametime} > \text{exposure time} + \text{read out time} \\ > T_{\text{Int}} + t_U([P_Y] * ([P_X] + LP) + LP + \text{CPRE})$$

with the boundary conditions:

$t_U$  = time unit in ns (50.00ns at 20.000MHz sensor clock)

$T_{\text{Int}}$  = exposure time (1  $\mu$ s - 0.5 s)

LP = line pause (8 ... 255)

CPRE = clocks after exposure of the sensor, CPRE = 42

$P_X$  = Number of pixels read out in the X direction (4..752) columns

$P_Y$  = Number of pixels read out in the Y direction (1..582) rows

If the line jump function is active, the number of lines read out will be reduced corresponding to the value of the line jump. Frame rate is the reciprocal of frame time. With an external clock MCLK, the time unit  $t_U$  must match the frequency used. A calculator for calculating frame rate is available at [www.photonfocus.com](http://www.photonfocus.com).

### 10.2.12 Register 33: Line jump (and pixel jump)

This register contains the value for the interlace mode. The line counter is incremented by this value. The lines in between are skipped. This mode is activated by setting bit 4 register 12. With row hopping, this value is also used to clock the DVAL signal.

### 10.2.13 Register 47: RAM-Bank selection

The RAM banks in the FPGA are selected with this register.

### 10.2.14 Registers 48-63: Data for 16x8 RAM-Banks

RAM banks have been implemented for internal parameters not used constantly by state machines. RAM-bank 0 is used for DAC-control.

## 10.3 Instructions for control of the Sensor Module

Table 20 shows the camera control commands.

**Table 20: Camera control commands**

C	Description
3	Execute EEPROM, start access to EEPROM and the corresponding operation.
4	Reset camera, reloads values from EEPROM

Abbreviations: C: Command

**10.4 Summary of the most important operation modes and their significance**
**Table 21: Overview of the operation modes**

<b>Operation mode</b>	<b>Description</b>
MCLK	Master clock: camera works with external clock generator. Used for synchronizing several camera systems
Exsync	External synchronization: camera is externally triggered and delivers image data in response to a trigger signal
CFR	Constant frame rate: ensures constant frame rate (data quantity), in that the camera delivers only a limited number of images/second (at constant exposure time). The number of images/second can be set
Skim-Mode	Skimming: increases small signal gain at sensor level and thus increases camera sensitivity
Flip Image	Turns image upside down
8 bit	Camera delivers 8 bit data (Gray levels 0..255)
LUT	Look-Up-Table: 9 bit sensor data are represented as 8 bits, using an LUT internal to the camera (freely selectable). Camera delivers 8 bit data (Gray levels 0..255)
LFSR	Linear-Feedback-Shift-Register: generates a pseudo-random image, so that errors can be identified in the complete image processing system
LOG-Mode	Pure logarithmic mode: the pixels function as simple photo-diodes and are continuously exposed to the light source. Because of the diode characteristics, the high gain mode must be active. With this mode, an FPN correction is necessary because variations in the pixel structures directly influence the image quality.
LinLog2-Mode	Linear-logarithmic mode: increases the image contrast by up to 120dB, without losing the advantages of a "Global Shutter"
HighGain	Gain 4: increases the gain in the analog path by a factor of 4 and thus makes the camera more sensitive
Linehopping (Zeilensprung)	Line jump: individual lines are selectively jumped over and not output. The maximum frame rate thus increases linearly.
Decimation	Pixels are jumped over in the x- and y-directions, in such a way that the image diagonal is retained
ROI	Region Of Interest: selected windows of the sensor are read out, reducing the quantity of data at constant resolution.
Linepause	A break in the clock cycles, occurring after the line has been output and before starting readout of the next line. Improves the image quality for non-centered ROI and allows adaptation to Frame grabber requirements

Full details of the various modes may be found in chapters 5 to 10.

## 11 Register assignment and instruction set of the ADC-Module

The LUT (look up table) of the ADC module can be modified via the RS232 interface. The communication is just like the sensor module's communication. To select the ADC module, one must write to register 0EH of the sensor module. Writing to this register again resets the flag, selecting the sensor module instead of the ADC module.

Table 22 shows the register assignment of the ADC module.

When the camera uses an external master clock MCLK, the ADC module is not accessible via the RS232 interface because the baud rate is directly derived from the PIXEL\_CLK. To circumvent this, the camera must first be set into the master mode. Afterwards the register and the LUT of the ADC module are accessible. After accessing the ADC module, the camera must be reset to slave mode, where the external clock is used.

**Table 22: Register 0 to 63 of the ADC-module**

REG DEC	REG HEX	W or C	Function during WRITE	R	Function during READ
0	0	W	Data EEPROM	R	Data EEPROM
1	1	W	LSB Address EEPROM	R	Cancel = 18H
2	2	W	MSB Address and OP-Code EEPROM	R	Cancel = 18H
3	3	C	SEND_PROM	R	Cancel = 18H
4	4	C	RELOAD of the internal register	R	Status3 Status for internal states
5	5	-	Not used	R	Cancel = 18H
6	6	W	Mode 0: Set mode ADC-Module	R	Settings and ADC-state
7	7	-	Not used	R	Cancel = 18H
8	8	W	Data RAM-LUT	R	Data RAM-LUT
9	9	W	LSB Address RAM-LUT	R	Cancel = 18H
10	A	W	MSB Address RAM-LUT	R	Cancel = 18H
11	B	-	Not used	R	Cancel = 18H
12	C	-	Not used	R	Cancel = 18H
13	D	-	Not used	R	Cancel = 18H
14	E	-	Register Slave/Master RS232, Switches between sensor or ADC module	R	Cancel = 18H
15	F	-	Not used	R	Cancel = 18H
16 - 63	10 - 3F	-	Not used	R	Cancel = 18H

Abbreviations:

R : Read

W : Write

C : Command

Cancel: Response value for access to an undefined register

## 11.1 Instructions for control of the ADC-Module

### 11.1.1 Register Addresses 0 – 3: EEPROM control

The EEPROM control is identical to the sensor module case. Appendix D describes the access of the EEPROM via the RS232 interface. The register assignments of the ADC module are shown in detail in Appendix B.

### 11.1.2 Register Address 4: Status information of the ADC-Module

The ADC module status is shown in status register 3 (see Table 23). Bit 2 is set to "1" and labels the ADC module. Bits 0 and 1 of status register 3 contain information about the state of the EEPROM when storing camera settings. If the camera is in the AUTOLOAD state (after power-on or reset of the camera), the settings are being copied from the EEPROM to the internal registers. **During this phase, EEPROM access is not permitted because otherwise incorrect information will get into the internal camera register.** The PROM\_BUSY state indicates an uncompleted writing cycle (active memory load) during write access to the EEPROM. **EEPROM access in this condition should always be avoided!**

**Table 23: Status register 3 (register address REGADDR = 4D = 04H)**

STATUS3_REG		
bit	Description	Default
0	AUTOLOAD, signalizes active Power-Up or Reload of data from EEPROM, write access forbidden	0
1	PROM_BUSY, write access forbidden	0
2	= 1, bit always high, coding for ADC module	1
3	Not used, arbitrary logical state	0
4	Not used, arbitrary logical state	0
5	Not used, arbitrary logical state	0
6	Not used, arbitrary logical state	0
7	Not used, arbitrary logical state	0

### 11.1.3 Register Address 6: Basic modes and ADC-condition

Bit 0 of the mode register must be set to 1 to access and modify the RAM-LUT via the registers 08H – 0AH. Bit 1 and bit 2 select the USER-LUT during the reload phase. To select for instance the USER-LUT1 into the RAM-LUT, bit 1 must be set, bit 2 must be reset and followed by a reload of the LUT.

**Table 24: Mode register 0 (Register address REGADDR = 6D = 06H)**

MODE0_REG			
bit	Name	Description	Default
0	R/W_LUT	= 1 → Enable Read/Write RAM-LUT	0
1	USER_LUT bit 0	Selection of one of four user LUT	0
2	USER_LUT bit 1		0
3	Not used	-	0
4	Not used	-	0
5	Not used	-	0
6	Not used	-	0
7	Not used	-	0

**Table 25: LUT selection**

USER_LUT bit 0	USER_LUT bit 1	Function	Description
0	0	LUT 0	Selects the first LUT
1	0	LUT 1	Selects the second LUT
0	1	LUT 2	Selects the third LUT
1	1	LUT 3	Selects the fourth LUT

## 11.2 Instructions for control of the ADC-Module

Table 26 displays the defined commands.

**Table 26: ADC-Module commands**

C	Description
3	Execute EEPROM, access to the EEPROM starts according selected operation
4	Reload LUT, LUT-Data is copied from the EEPROM into the RAM-LUT

Abbreviation:

C: Command

## 12 Cleaning the sensor

**As a matter of principle, the camera should only be cleaned in ESD-safe areas.** The person performing the cleaning must also be **earthed** by means of a **wrist strap!**

Dust or loose particles should be removed by using clean compressed air (e.g. Electrolube EAD400D compressed air spray) with a maximum pressure of 5 Bar.

First remove coarse particles and dirt from the sensor using Q-Tips soaked in 2-propanol, applying as little pressure as possible. Using a method similar to that used for cleaning optical surfaces, clean the sensor by starting at any corner of the sensor and working towards the opposite corner. Finally, repeat the procedure with methanol to remove streaks.

**It is imperative that no pressure be applied to the surface of the sensor or to the Globe-Top surrounding the optically active surface during the cleaning process. The use of pointed or sharp objects during the cleaning of the sensor will lead to irreversible damage to the sensor.**

To clean the sensor, employ Q-Tips used for cleaning semiconductors and optical surfaces, together with the following organic solvents:

Q-Tips:

Sharp Point Slim HUBY-340  
Large Q-Tips SWABS CA-003  
Small Q-Tips SWABS BB-003

Available from:

German supplier:  
Hans J. Michael GmbH  
Aspacher Str. 15-17  
D-71522 Backnang Deutschland

Organic cleaning liquids:

Methanol Semiconductor Grade 99.9% min (Assay)  
Merk 12,6024, UN1230, slightly flammable and **poisonous**

2-Propanol (ISO-Propanol) Semiconductor Grade 99.5% min (Assay)  
Merk 12,5227, UN1219, slightly flammable

Supplier:

Alfa Aesar  
Johnson Matthey GmbH  
Zeppelinstr. 7  
D-76185 Karlsruhe Deutschland  
[www.alfa-chemcat.com](http://www.alfa-chemcat.com)

## 13 Appendix A – Configuration Settings of the EEPROM Sensor Module

The configuration EEPROM of the sensor module contains data for the configuration of the module and a storage facility for the variables of the software, which are used to control the camera settings and the camera characteristics. Table 27 shows the storage functions of the EEPROM.

**Table 27: Functions of the 2kB storage facility of the configuration EEPROM**

Storage Address	Description	Reference
000H	EEPROM size	Default 06H
001H - 1FFH	Factory settings = booting data for the hardware	Table 28
200H - 3FFH	Copy of the factory settings	Table 28
400H - 4FFH	Storage for trimming values of the auxiliary sensor voltages	Table 29 and Table 30
500H - 6FFH	Main memory for software amendments	Software manual [SOFT]
700H - 7FFH	reserved	-

The stored data in address 000H of the EEPROM describes the storage capacity. It is used for the recognition of a chosen configuration.

Subsequently the byte 00H is the factory setting in the EEPROM. The factory settings contain all parameters which are needed for the operation of the camera after power up or reset. Table 28 shows the EEPROM addresses and the corresponding FPGA internal register addresses. Some default values are dependent on the individual fine-tuning of the camera so these values are only recommended starting values.

An copy of the factory settings, including the EEPROM size is deposited in the address 200H – 3FFH, thus enabling a restoration of the camera settings by software. Nevertheless, it is recommended that the user saves a copy of the factory settings on an external storage medium.

In the addresses 400H – 4FFH there are complete sets of DAC values for 8 operating modes. Table 27 shows the basic addresses for the sets. Table 28 shows the individual DAC channels with their corresponding register values.

The storage addresses 500H – 6FFH are reserved for camera control variables. Details can be found in the software manual.

The area 700H – 7FFH is reserved.

In the event of queries or service requests, a dump of the EEPROM contents should be sent to Photonfocus together with an error description.

**Table 28: EEPROM Functions and Assignment to internal FPGA register**

Name	Description	R/W or C	PROM Address	FPGA Register Address	Default
			HEX	HEX	HEX
EEPROM	EEPROM size	-	0	-	06
MODE0[7:0]	Mode register 0	R/W	1	6	01
MODE1[7:0]	Mode register 1	R/W	2	7	16
Sys_Ctl_LSB	LSB DAC0 System Control Register	W	3	8	60
Sys_Ctl_MSB	MSB DAC0 System Control Register	W	4	9	00
Chan0_Ctl_LSB	LSB DAC0 Channel Register 0	W	5	8	10
Chan0_Ctl_MSB	MSB DAC0 Channel Register 0	W	6	9	42
Chan1_Ctl_LSB	LSB DAC0 Channel Register 1	W	7	8	10
Chan1_Ctl_MSB	MSB DAC0 Channel Register 1	W	8	9	46
Chan2_Ctl_LSB	LSB DAC0 Channel Register 2	W	9	8	10
Chan2_Ctl_MSB	MSB DAC0 Channel Register 2	W	A	9	4A
Chan3_Ctl_LSB	LSB DAC0 Channel Register 3	W	B	8	10
Chan3_Ctl_MSB	MSB DAC0 Channel Register 3	W	C	9	4E
Chan4_Ctl_LSB	LSB DAC0 Channel Register 4	W	D	8	10
Chan4_Ctl_MSB	MSB DAC0 Channel Register 4	W	E	9	52
Chan5_Ctl_LSB	LSB DAC0 Channel Register 5	W	F	8	10
Chan5_Ctl_MSB	MSB DAC0 Channel Register 5	W	10	9	56
Chan6_Ctl_LSB	LSB DAC0 Channel Register 6	W	11	8	10
Chan6_Ctl_MSB	MSB DAC0 Channel Register 6	W	12	9	5A
Chan7_Ctl_LSB	LSB DAC0 Channel Register 7	W	13	8	10
Chan7_Ctl_MSB	MSB DAC0 Channel Register 7	W	14	9	5E
Chan0_Main_LSB	LSB DAC0 Channel 0 Main register	W	15	8	D7 (**)
Chan0_Main_MSB	MSB DAC0 Channel 0 Main register	W	16	9	20 (**)
Chan0_Sub_LSB	LSB DAC0 Channel 0 Sub register	W	17	8	00 (**)
Chan0_Sub_MSB	MSB DAC0 Channel 0 Sub register	W	18	9	A0 (**)
Chan1_Main_LSB	LSB DAC0 Channel 1 Main register	W	19	8	93 (**)
Chan1_Main_MSB	MSB DAC0 Channel 1 Main register	W	1A	9	27 (**)
Chan1_Sub_LSB	LSB DAC0 Channel 1 Sub register	W	1B	8	00 (**)
Chan1_Sub_MSB	MSB DAC0 Channel 1 Sub register	W	1C	9	A4 (**)
Chan2_Main_LSB	LSB DAC0 Channel 2 Main register	W	1D	8	2C (**)
Chan2_Main_MSB	MSB DAC0 Channel 2 Main register	W	1E	9	29 (**)
Chan2_Sub_LSB	LSB DAC0 Channel 2 Sub register	W	1F	8	00 (**)
Chan2_Sub_MSB	MSB DAC0 Channel 2 Sub register	W	20	9	A8 (**)
Chan3_Main_LSB	LSB DAC0 Channel 3 Main register	W	21	8	FF (**)
Chan3_Main_MSB	MSB DAC0 Channel 3 Main register	W	22	9	2F (**)
Chan3_Sub_LSB	LSB DAC0 Channel 3 Sub register	W	23	8	00 (**)
Chan3_Sub_MSB	MSB DAC0 Channel 3 Sub register	W	24	9	AC (**)

**Abbreviations:**

R: Read  
 W: Write  
 C: Command  
 DEC: Decimal value  
 HEX: Hexadecimal value  
 (\*): bit 2 to bit 7 arbitrary value  
 (\*\*): adjusted value

**Table 28(continuation): EEPROM Functions and Assignment to internal FPGA register**

Name	Description	R/ W or C	PROM Address	FPGA Register Address	Default
			HEX	HEX	HEX
Chan4_Main_LSB	LSB DAC0 Channel 4 Main register	W	25	8	00 (**)
Chan4_Main_MSB	MSB DAC0 Channel 4 Main register	W	26	9	30 (**)
Chan4_Sub_LSB	LSB DAC0 Channel 4 Sub register	W	27	8	00 (**)
Chan4_Sub_MSB	MSB DAC0 Channel 4 Sub register	W	28	9	B0 (**)
Chan5_Main_LSB	LSB DAC0 Channel 5 Main register	W	29	8	94 (**)
Chan5_Main_MSB	MSB DAC0 Channel 5 Main register	W	2A	9	36 (**)
Chan5_Sub_LSB	LSB DAC0 Channel 5 Sub register	W	2B	8	00 (**)
Chan5_Sub_MSB	MSB DAC0 Channel 5 Sub register	W	2C	9	B4 (**)
Chan6_Main_LSB	LSB DAC0 Channel 6 Main register	W	2D	8	47 (**)
Chan6_Main_MSB	MSB DAC0 Channel 6 Main register	W	2E	9	39 (**)
Chan6_Sub_LSB	LSB DAC0 Channel 6 Sub register	W	2F	8	00 (**)
Chan6_Sub_MSB	MSB DAC0 Channel 6 Sub register	W	30	9	B8 (**)
Chan7_Main_LSB	LSB DAC0 Channel 7 Main register	W	31	8	FF (**)
Chan7_Main_MSB	MSB DAC0 Channel 7 Main register	W	32	9	3F (**)
Chan7_Sub_LSB	LSB DAC0 Channel 7 Sub register	W	33	8	FF (**)
Chan7_Sub_MSB	MSB DAC0 Channel 7 Sub register	W	34	9	BF (**)
MODE2[7:0]	Mode register 2	R/W	35	C	42
MODE3[7:0]	Mode register 3	R/W	36	D	20
MODE4[7:0]	Mode register 4	R/W	37	E	00
EXPOSURE_TIME[7:0]	LSB Exposure time	R/W	38	F	E0
EXPOSURE_TIME[15:8]	MSB-1 Exposure time	R/W	39	10	93
EXPOSURE_TIME[23:16]	MSB Exposure time	R/W	3A	11	04
LINLOG_TIME[7:0]	LSB LinLog Time	R/W	3B	12	80
LINLOG_TIME[15:8]	MSB-1 LinLog Time	R/W	3C	13	A9
LINLOG_TIME[23:16]	MSB LinLog Time	R/W	3D	14	03
FRAME_PAUSE[7:0]	LSB Frame pause	R/W	3E	15	FF
FRAME_PAUSE[15:8]	MSB-1 Frame pause	R/W	3F	16	FF
FRAME_PAUSE[23:16]	MSB Frame pause	R/W	40	17	1F
X0_ROI[7:0]	LSB ROI-X0 Matrix sensors	R/W	41	18	00
X0_ROI[15:8]	MSB ROI-X0 Matrix sensors (*)	R/W	42	19	00
Y0_ROI[7:0]	LSB ROI-Y0 Matrix sensors	R/W	43	1A	00
Y0_ROI[15:8]	MSB ROI-Y0 Matrix sensors (*)	R/W	44	1B	00
X1_ROI[7:0]	LSB ROI-X1 Matrix sensors	R/W	45	1C	FF
X1_ROI[15:8]	MSB ROI-X1 Matrix sensors (*)	R/W	46	1D	FF
Y1_ROI[7:0]	LSB ROI-Y1 Matrix sensors	R/W	47	1E	FF
Y1_ROI[15:8]	MSB ROI-Y1 Matrix sensors (*)	R/W	48	1F	FF
LINE_PAUSE[7:0]	Line pause	R/W	49	20	08
ZEILENSPRUNG[7:0]	Line jump	R/W	4A	21	02
X_OFF[7:0]	Offset parameter in x direction	R/W	4B	22	88
Not used	-	R/W	4C	23	FF
Y_OFF[7:0]	Offset parameter in y direction	R/W	4D	24	DD
Not used	-	R/W	4E	25	FF
Not used	-	R/W	4F	26	FF
Not used	-	R/W	50	27	FF
Not used	-	R/W	51	28	FF
Not used	-	R/W	52	29	FF
Not used	-	R/W	53	2A	FF
Not used	-	R/W	54	2B	FF
Not used	-	R/W	55	2C	FF
Not used	-	R/W	56	2D	FF
Not used	-	R/W	57	2E	FF
RAM_BANK_SELECT[7:0]	RAM Bank Selection	R/W	58	2F	00

**Table 28 (continuation): EEPROM Functions and Assignment to internal FPGA register**

Name	Description	R/ W or C	PROM Address	FPGA Register Address	Default
			HEX	HEX	HEX
BANK0_BYTE0[7:0]	Global Offset Low Gain LSB	R/W	5D	30	94 (**)
BANK0_BYTE1[7:0]	Global Offset Low Gain MSB	R/W	5E	31	36 (**)
BANK0_BYTE2[7:0]	Global Offset High Gain LSB	R/W	5F	32	83 (**)
BANK0_BYTE3[7:0]	Global Offset High Gain MSB	R/W	60	33	37 (**)
BANK0_BYTE4[7:0]	No LinLog LSB (LL2)	R/W	61	34	00 (**)
BANK0_BYTE5[7:0]	No LinLog MSB (LL2)	R/W	62	35	30 (**)
BANK0_BYTE6[7:0]	Log Parameter LSB	R/W	63	36	F4 (**)
BANK0_BYTE7[7:0]	Log Parameter MSB	R/W	64	37	31 (**)
BANK0_BYTE8[7:0]	LinLog Parameter LSB (LL1)	R/W	65	38	BC (**)
BANK0_BYTE9[7:0]	LinLog Parameter MSB (LL1)	R/W	66	39	32 (**)
BANK0_BYTE10[7:0]	No Skimming LSB	R/W	67	3A	FF (**)
BANK0_BYTE11[7:0]	No Skimming MSB	R/W	68	3B	2F (**)
BANK0_BYTE12[7:0]	Skimming 0 LSB (1.40V factory setting)	R/W	69	3C	58 (**)
BANK0_BYTE13[7:0]	Skimming 0 MSB	R/W	6A	3D	2E (**)
BANK0_BYTE14[7:0]	Skimming 1 LSB (1.18V factory setting)	R/W	6B	3E	F4 (**)
BANK0_BYTE15[7:0]	Skimming 1 MSB	R/W	6C	3F	2D (**)

**Abbreviations:**

R: Read  
 W: Write  
 C: Command  
 DEC: Decimal value  
 HEX: Hexadecimal value  
 (\*): bit 2 to bit 7 arbitrary value  
 (\*\*): adjusted value

**Table 29: Basic addresses of the DAC values for 8 operating modes**

Basic Addresses HEX	Extended Operating Mode	Description
400	TBD	-
420	TBD	-
440	TBD	-
460	TBD	-
480	TBD	-
4A0	TBD	-
4C0	TBD	-
4E0	TBD	-

**Table 30: Assignment of the DAC values to storage values**

EEPROM Address HEX	DAC Functions and Operating Modes
Base + 00	LSB DAC0 Channel 0 Main register
Base + 01	MSB DAC0 Channel 0 Main register
Base + 02	LSB DAC0 Channel 0 Sub register
Base + 03	MSB DAC0 Channel 0 Sub register
Base + 04	LSB DAC0 Channel 1 Main register
Base + 05	MSB DAC0 Channel 1 Main register
Base + 06	LSB DAC0 Channel 1 Sub register
Base + 07	MSB DAC0 Channel 1 Sub register
Base + 08	LSB DAC0 Channel 2 Main register
Base + 09	MSB DAC0 Channel 2 Main register
Base + 0A	LSB DAC0 Channel 2 Sub register
Base + 0B	MSB DAC0 Channel 2 Sub register
Base + 0C	LSB DAC0 Channel 3 Main register
Base + 0D	MSB DAC0 Channel 3 Main register
Base + 0E	LSB DAC0 Channel 3 Sub register
Base + 0F	MSB DAC0 Channel 3 Sub register
Base + 10	LSB DAC0 Channel 4 Main register
Base + 11	MSB DAC0 Channel 4 Main register
Base + 12	LSB DAC0 Channel 4 Sub register
Base + 13	MSB DAC0 Channel 4 Sub register
Base + 14	LSB DAC0 Channel 5 Main register
Base + 15	MSB DAC0 Channel 5 Main register
Base + 16	LSB DAC0 Channel 5 Sub register
Base + 17	MSB DAC0 Channel 5 Sub register
Base + 18	LSB DAC0 Channel 6 Main register
Base + 19	MSB DAC0 Channel 6 Main register
Base + 1A	LSB DAC0 Channel 6 Sub register
Base + 1B	MSB DAC0 Channel 6 Sub register
Base + 1C	LSB DAC0 Channel 7 Main register
Base + 1D	MSB DAC0 Channel 7 Main register
Base + 1E	LSB DAC0 Channel 7 Sub register
Base + 1F	MSB DAC0 Channel 7 Sub register

## 14 Appendix B - The configuration EEPROM ADC Module and its functions

The configuration EEPROM of the ADC module contains four 512Byte sized look-up tables (LUT). With these LUT tables it is possible to transform 9bit ADC values into 8bit values for the camera interface. This transformation is managed by directly addressing one 512Byte LUT, whose 8bit interface is directly linked with the camera interface. When the camera is powered up, the internal RAM-LUT is loaded with the values of LUT0. The values of the LUT1, LUT2 or LUT3 can be copied in the RAM-LUT by setting the selection bits for these LUTs and subsequently reloading.

The LUT tables are preprogrammed when the camera is delivered. The LUT can be changed by the user through the RS232 interface. To change the default settings, user values can be stored in the EEPROM.

The EEPROM is divided into four areas as shown in Table 31. The address values in the EEPROM correspond to the addresses of the RAM-LUT in the ADC module. With LUT 1 the EEPROM address 200H corresponds to the LUT address 000H and so on.

**Table 31: EEPROM address separation EEPROM 9386**

Address	Description
000H - 1FFH	Data for User-LUT0 LUT 9 to 8 bit
200H - 3FFH	Data for User-LUT1 LUT 9 to 8 bit
400H - 5FFH	Data for User-LUT2 LUT 9 to 8 bit
600H - 7FFH	Data for User-LUT3 LUT 9 to 8 bit

## 15 Appendix C - RS232 Interface

The RS232 interface is a three-lead-interface (RX, TX, GND). This interface is often used in industrial image processing for controlling camera settings. The cameras from Photonfocus have an RS232 compatible interface. The following communication settings from the RS232 protocol have been chosen for the Photonfocus camera series:

Baud rate	9600
Start bit	1
data bits	8
Parity	none
Stop bit	1

Through the selection of 8 data bits, it is possible to read one data byte with a single shot. In the idle state the leads RX and TX are characterized by a **standard H-level**. Data transfer begins with a **start bit**, which has a **L-level**. Afterwards the 8 data bits are transmitted in the **sequence from D0...D7**. In order to separate subsequent data a stop bit of **H-level** is added. The total number of cycles necessary for data transfer is 10. After the data transfer, signals return to the idle state.

### 15.1 Definition of the transfer protocol

Due to the 8 bit RS232 limitation, it is not possible to distinguish between data and address transfers. The protocol in Table 32 is implemented to allow access to the 64 internal camera registers.

**Table 32: Communication protocol**

RS232 Communication Protocol	Data bits							
	7	6	5	4	3	2	1	0
Command to camera controller	0	1	A5	A4	A3	A2	A1	A0
WRITE Address	0	1	A5	A4	A3	A2	A1	A0
WRITE Data Low Nibble	1	0	x	x	D3	D2	D1	D0
WRITE Data High Nibble	1	1	x	x	D7	D6	D5	D4
READ Data of Addresses	0	0	A5	A4	A3	A2	A1	A0

X: don't care  
 Ai: Address bits  
 Dj: Data bits

When data or addresses are written (WRITE Mode), the RS232 interface of the camera answers with ACK = 06H, if the transfer was successful, or with NAK = 15H if the transfer failed. Therefore it is possible to control the complete transfer process by the software. When a register is read, the desired data is transmitted as a complete byte in order to accelerate communication. Faulty data transmissions can only be recognized using the stop bit. Additionally there are internal status registers (in the camera) which record failures during transmission. An attempt to access an undefined camera register will be answered with CAN = 18H. An overview over the camera feedback is shown in Table 33.

**Table 33: Camera feedbacks**

Camera Feedback	Abbreviation	Code
Successful transfer	ACK	06H
Failed transfer	NAK	15H
Undefined access	CAN	18H
Camera data	DATA	xxH

x: arbitrary data

## 15.2 Example of access to camera registers

For data transmission to the camera, the camera must be slave, and the PC must be master. The camera receives data on the RX lead and transmits data to the PC via the TX lead.

Table 34 summarizes the individual steps of a write/read of the register 06H and 07H from the master's point of view. Additionally a read process of an undefined register 16H is shown.

**Table 34: Accessing camera registers**

Steps	RX/TX	BIN Code	HEX Code	Comments
1	RX	0100 0110	46	Write address 06H in the address register of the camera
2	TX	0000 0110	06	Successful receipt, camera transmits ACK = 06H
3	RX	1000 0101	85	Write Low Data Nibble 5
4	TX	0000 0110	06	Successful receipt, camera transmits ACK = 06H
5	RX	1100 0101	C5	Write High Data Nibble 5
6	TX	0000 0110	06	Successful receipt, camera transmits ACK = 06H
7	RX	0100 0111	47	Write address 07H in the address register of the camera
8	TX	0000 0110	06	Successful receipt, camera transmits ACK = 06H
9	RX	1000 1010	8A	Write Low Data Nibble A
10	TX	0001 0101	15	Failed transfer, Master must repeat transfer, camera transmits NAK = 15H
11	RX	1000 1010	8A	Write Low Data Nibble A
12	TX	0000 0110	06	Successful receipt, camera transmits ACK = 06H
13	RX	1100 1010	CA	Write High Data Nibble A
14	TX	0000 0110	06	Successful receipt, camera transmits ACK = 06H
15	RX	0000 0110	06	Read Data from register address 6
16	TX	0101 0101	55	camera transmits register content address 06H → 55H
17	RX	0000 0111	07	Read data from register address 7
18	TX	1010 1010	AA	camera transmits register content address 07H → AAH
19	RX	0001 0111	16	Read data from undefined register address 16H
20	TX	0001 1000	18	camera transmits CAN = 18H; not allowed or undefined

## 16 Appendix D – Accessing the EEPROM

The first 4 registers are used for the communication with the configuration EEPROM of the camera. Register address 0 contains the data, which are written to or read from the EEPROM. The register 1 contains the LSB of the storage address. The register 2 contains the MSB of the storage address as well as the accessing code (OP code) for the EEPROM. The configuration EEPROM has a storage capacity of 2 kB. Therefore the valid storage addresses are 11 bits (A0 – A10) and range from 000H to 7FFH. After entering the data, the address and the OP code, all this information is transferred to the EEPROM with the command SEND\_PROM (write register address 3). To read bytes from the EEPROM, the address and the OP code have to be transferred with the command SEND\_PROM to the EEPROM. The result can then read from register address 0. An overview of the registers that are used for the EEPROM programming is shown in Table 35.

In order to be able to write to the EEPROM, the write protection must be disabled. The PROM\_BUSY and the AUTOLOAD flag in the EEPROM register address 4 bit 1 or bit 0 must also be checked before writing to the EEPROM. Writing during the BUSY phase leads to malfunctions of the camera. After writing, the write protection should be enabled again. This happens automatically when the camera is switched off or loses power.

**Table 35: Overview of the register, which are used for the EEPROM programming**

Register address 0 - DATA_EEPROM		
bit	Name	Description
0 -7	DATA_EEPROM	Data bit 0 – 7

Register address 1 - ADDR_LSB_EEPROM		
bit	Name	Description
0 - 7	ADDR_LSB_EEPROM	Address bit 0 – 7

Register address 2 - ADDR_MSB_EEPROM		
bit	Name	Description
0	ADDR_MSB_EEPROM	Address bit 8
1	ADDR_MSB_EEPROM	Address bit 9 / OP-Code bit 0
2	ADDR_LSB_EEPROM	Address bit 10 / OP-Code bit 1
3	ADDR_LSB_EEPROM	OP-Code bit 2
4	ADDR_LSB_EEPROM	OP-Code bit 3
5	Not used	-
6	Not used	-
7	Not used	-

Command	bit 4	bit 3	bit 2	bit 1	bit 0
Read	1	0	A10	A9	A8
Write	0	1	A10	A9	A8
Write disable	0	0	0	0	X
Write enable	0	0	1	1	X

### Abbreviations

0: Logical state 0  
 1: Logical state 1  
 X: arbitrary state

### 16.1 Example of EEPROM access

Table 36 summarizes the sequence of commands for data transmission to the EEPROM of the camera. Depending on the access function, some steps may not be necessary. To write to the EEPROM, steps 1-5 are necessary. To read, skip step 1, but use steps 2-7. Special cases are the EEPROM commands write enable/disable. In these cases only the steps 3-5 have to be used. The transmission protocol of the RS232 interface is defined in Appendix C.

**Table 36: Access steps for the EEPROM**

Step	Action
1	Write data byte (D7-D0) in register address 00H, if required for function
2	Write LSB address byte (A7-A0) in register address 01H, if required for function
3	Write OP-Code und MSB address byte (xxx,OP1, OP2,A10-A8) in register address 02H
4	Read status register address 04H, wait for state „not (PROM_BUSY or AUTOLOAD)“
5	Write in register address 03H → command SEND_PROM
6	Read status register address 04H, wait for state „not (PROM_BUSY or AUTOLOAD)“
7	Read data byte (D7-D0) in register address 00H, when data are read out from the EEPROM

The following example Table 37 shows in detail the sequence of commands for the EEPROM command write enable.

**Table 37: Example accessing the EEPROM with the command „WRITE ENABLE“**

Step	BIN Code	HEX Code	Comments
1	-	-	<b>These steps are not required</b>
2	-	-	
3	xxx0 0xxx	06	OP-Code = 00 (2-bits)
	xxxx x11x		Extended OP code A10..A8 = 11x (3-bits)
	0000 0110		Write OP-Code in register address 02H
4	00xx xxxx	04	READ from address
	xx00 0100		Address 04H
	0000 0100		Read status register from register address 04H
5	01xx xxxx	43	Write to address
	xx00 0011		Address 03H
	0100 0011		Command SEND_PROM, Data will be transmitted to the EEPROM
6	-	-	<b>These steps are not required</b>
7	-	-	

x: arbitrary state

## 17 Appendix E – How to handle the DAC?

The camera is trimmed by the digital-analog-converter (DAC). The DAC can be directly programmed via the RS232 interface of the camera. During reset or power up, the DAC receives the data stored in the configuration EEPROM. The RS232 interface requires transmitting a double byte (16bit value), where the LSB has to be written in the register address 08H and the MSB in the register 09H of the camera. After the MSB transmission the DAC is automatically addressed. **It is not possible to read back any settings from the DAC.**

The DAC properties are determined by the system register (system control) where the properties of each single channel can be specified by channel register (channel control). Every DAC channel has a main register and a sub register. The main register value is a rough or coarse adjustment of the DAC output voltage and the sub register value is a fine adjustment of the same DAC output voltage.

The individual control parameters are shown in the Table 38.

**Table 38: Individual control parameters**

BIT:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
System-control	X	0	0	X	X	X	X	X	0	BIN	PD	SSTBY	SCLR	0	X	X
Channel-control	X	1	0	A2	A1	A0	MX1	MX0	X	X	X	STBY	CLR	0	X	X
Main-Register	0	X	1	A2	A1	A0	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Sub - Register	1	X	1	A2	A1	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	X	X

BIN: coding method (0 = two's compliment or 1 = binary with offset)  
 PD: Power Down (0 = Power Down)  
 SSTBY: System Stand by (1= Stand by)  
 SCLR: System Clear (1 = deletes the DAC Outputs)  
 STBY: Channel Standby (0 = Stand by)  
 CLR: Software Clear (1 = Clear)  
 A2..A0: addresses for selecting the channel (0..7)  
 DB9..DB0: data for rough and fine adjustment  
 MX1, MX0: Selection of the reference source  
           00: Vbias= VDD/2 = 1.65V  
           01: Vbias= internal reference Vref = 1.23V  
           10: Vbias= external reference Vref = 1.25V  
           11: not determined  
 0: logical state 0  
 1: logical state 1  
 X: arbitrary logical state

The system register and the channel register are preprogrammed according to the factory settings after power up or reset of the camera and should not be changed. Any changes of these values lead to malfunctions of the camera and can also **damage the CMOS sensor**. Table 39 shows the factory settings of the system and the channel register and their function.

**Table 39: Factory settings of the system register and the channel register**

DAC Register	HEX Code	Description
System register	0060	Coding method, binary with offset
Channel register 0	4210	Active output, external reference Vref = 1.25V
Channel register 1	4610	Active output, external reference Vref = 1.25V
Channel register 2	4A10	Active output, external reference Vref = 1.25V
Channel register 3	4E10	Active output, external reference Vref = 1.25V
Channel register 4	5210	Active output, external reference Vref = 1.25V
Channel register 5	5610	Active output, external reference Vref = 1.25V
Channel register 6	5A10	Active output, external reference Vref = 1.25V
Channel register 7	5E10	Active output, external reference Vref = 1.25V

The output voltage is determined by the following equation:

$$V_{out} = V_{bias} * (1 + 1.875 * (NA - 512) / 1024 + (NB - 128) / 4096) ,$$

*V<sub>out</sub>*: the desired output voltage,

*V<sub>bias</sub>*: the reference voltage ( $V_{DD}/2$ , internal  $V_{REF} = 1.23$  V or external  $V_{Ref} = 1.25$  V),

NA: the decimal value for the main register,

NB: the decimal value for the sub-register.

If NB is set to  $NB = 128$  NA can be determined from *V<sub>out</sub>* as follows:

$$NA = \frac{V_{out} - V_{bias}}{1.875 * V_{bias}} * 1024 + 512 .$$

The storage addresses for the individual register values in the EEPROM are available in the appendix A. Power up values and extended operating mode values are not the same. With Photonfocus' software library the voltage values corresponding to the individual operating modes can be stored in the EEPROM after fine tuning.

## 18 Appendix F – Pseudo random number generator

In order to test the interface between camera and frame grabber a 8bit LFSR (linear feedback shift register) with a "many-to-one" feedback structure has been implemented [SMITH00]. For a maximum sequence length of 255 states, an XOR feedback at tap 0 and 6 was implemented (VHDL implementation, see below). The state 0 does not exist in this implementation. The sequence starts with the value 1 at the beginning of every line. The 255 states are shown in Table 40. The result is a pattern of vertical stripes in the captured picture (see Fig. 14).

**Table 40: States 0 – 127 of the pseudo random number generator**

Nr.	HEX	BIN	Nr.	HEX	BIN	Nr.	HEX	BIN	Nr.	HEX	BIN
0	01	10000000	32	21	10000100	64	C5	10100011	96	DD	10111011
1	02	01000000	33	42	01000010	65	8A	01010001	97	BB	11011101
2	05	10100000	34	85	10100001	66	15	10101000	98	77	11101110
3	0B	11010000	35	0A	01010000	67	2B	11010100	99	EE	01110111
4	16	01101000	36	14	00101000	68	56	01101010	100	DC	00111011
5	2C	00110100	37	29	10010100	69	AC	00110101	101	B9	10011101
6	58	00011010	38	53	11001010	70	59	10011010	102	72	01001110
7	B1	10001101	39	A7	11100101	71	B3	11001101	103	E5	10100111
8	63	11000110	40	4F	11110010	72	66	01100110	104	CA	01010011
9	C7	11100011	41	9F	11111001	73	CC	00110011	105	95	10101001
10	8F	11110001	42	3E	01111100	74	99	10011001	106	2A	01010100
11	1E	01111000	43	7D	10111110	75	32	01001100	107	54	00101010
12	3D	10111100	44	FA	01011111	76	65	10100110	108	A9	10010101
13	7A	01011110	45	F5	10101111	77	CB	11010011	109	52	01001010
14	F4	00101111	46	EA	01010111	78	97	11101001	110	A5	10100101
15	E8	00010111	47	D5	10101011	79	2F	11110100	111	4A	01010010
16	D0	00001011	48	AA	01010101	80	5F	11111010	112	94	00101001
17	A1	10000101	49	55	10101010	81	BF	11111101	113	28	00010100
18	43	11000010	50	AB	11010101	82	7E	01111110	114	51	10001010
19	87	11100001	51	57	11101010	83	FD	10111111	115	A2	01000101
20	0F	11110000	52	AE	01110101	84	FB	11011111	116	44	00100010
21	1F	11111000	53	5C	00111010	85	F7	11101111	117	89	10010001
22	3F	11111100	54	B8	00011101	86	EF	11110111	118	12	01001000
23	7F	11111110	55	70	00001110	87	DE	01111011	119	25	10100100
24	FF	11111111	56	E0	00000111	88	BC	00111101	120	4B	11010010
25	FE	01111111	57	C1	10000011	89	79	10011110	121	96	01101001
26	FC	00111111	58	83	11000001	90	F3	11001111	122	2D	10110100
27	F9	10011111	59	06	01100000	91	E6	01100111	123	5A	01011010
28	F2	01001111	60	0C	00110000	92	CD	10110011	124	B4	00101101
29	E4	00100111	61	18	00011000	93	9B	11011001	125	68	00010110
30	C8	00010011	62	31	10001100	94	37	11101100	126	D1	10001011
31	90	00001001	63	62	01000110	95	6E	01110110	127	A3	11000101

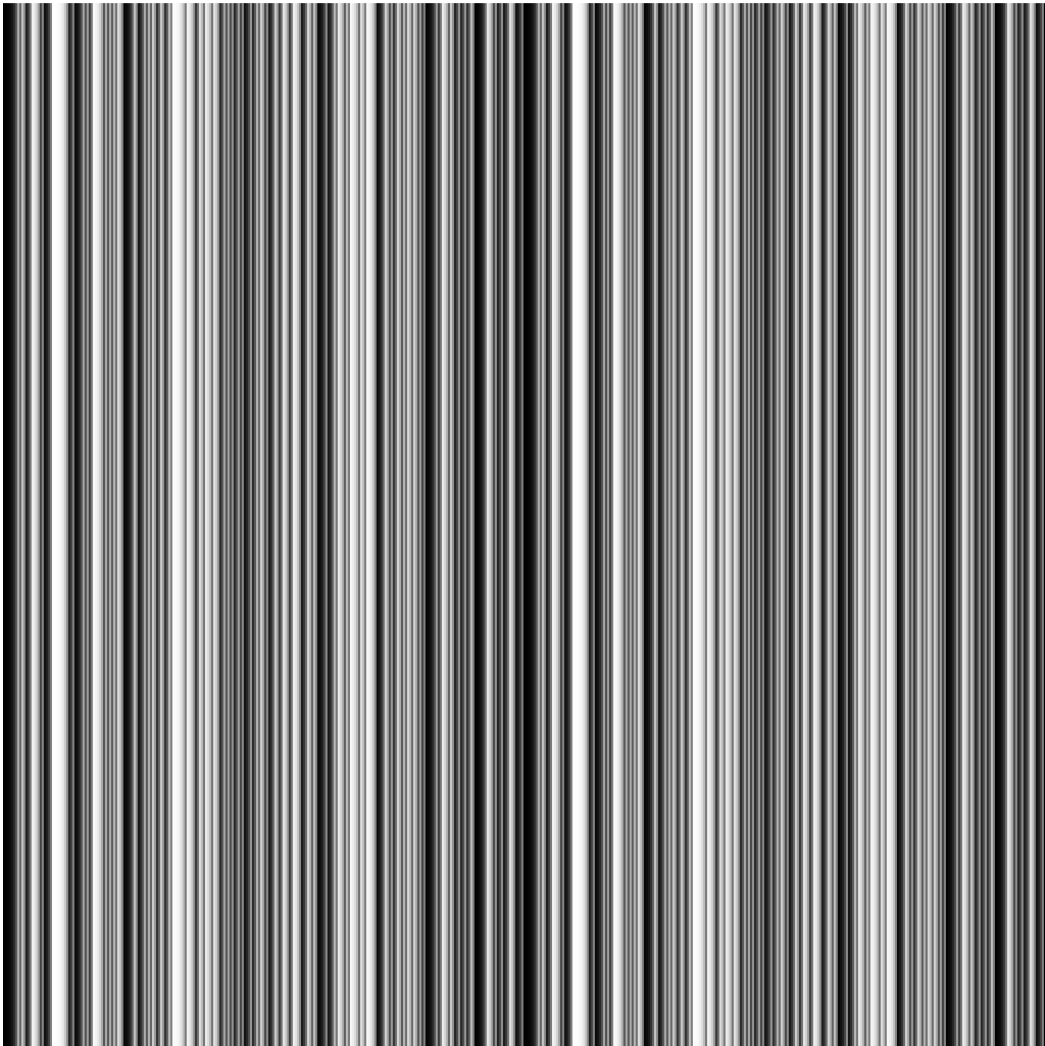
HEX: Hexadecimal value

BIN: Binary value, bit order 0 - 7

**Continuation of Table 40: States 128 – 255 of the pseudo random number generator**

Nr.	HEX	BIN	Nr.	HEX	BIN	Nr.	HEX	BIN	Nr.	HEX	BIN
128	46	01100010	160	2E	01110100	192	6B	11010110	224	26	01100100
129	8C	00110001	161	5D	10111010	193	D6	01101011	225	4C	00110010
130	19	10011000	162	BA	01011101	194	AD	10110101	226	98	00011001
131	33	11001100	163	75	10101110	195	5B	11011010	227	30	00001100
132	67	11100110	164	EB	11010111	196	B6	01101101	228	60	00000110
133	CE	01110011	165	D7	11101011	197	6D	10110110	229	C0	00000011
134	9C	00111001	166	AF	11110101	198	DA	01011011	230	81	10000001
135	39	10011100	167	5E	01111010	199	B5	10101101	231	03	11000000
136	73	11001110	168	BD	10111101	200	6A	01010110	232	07	11100000
137	E7	11100111	169	7B	11011110	201	D4	00101011	233	0E	01110000
138	CF	11110011	170	F6	01101111	202	A8	00010101	234	1D	10111000
139	9E	01111001	171	ED	10110111	203	50	00001010	235	3A	01011100
140	3C	00111100	172	DB	11011011	204	A0	00000101	236	74	00101110
141	78	00011110	173	B7	11101101	205	41	10000010	237	E9	10010111
142	F1	10001111	174	6F	11110110	206	82	01000001	238	D2	01001011
143	E3	11000111	175	DF	11111011	207	04	00100000	239	A4	00100101
144	C6	01100011	176	BE	01111101	208	09	10010000	240	48	00010010
145	8D	10110001	177	7C	00111110	209	13	11001000	241	91	10001001
146	1B	11011000	178	F8	00011111	210	27	11100100	242	23	11000100
147	36	01101100	179	F0	00001111	211	4E	01110010	243	47	11100010
148	6C	00110110	180	E1	10000111	212	9D	10111001	244	8E	01110001
149	D8	00011011	181	C3	11000011	213	3B	11011100	245	1C	00111000
150	B0	00001101	182	86	01100001	214	76	01101110	246	38	00011100
151	61	10000110	183	0D	10110000	215	EC	00110111	247	71	10001110
152	C2	01000011	184	1A	01011000	216	D9	10011011	248	E2	01000111
153	84	00100001	185	34	00101100	217	B2	01001101	249	C4	00100011
154	08	00010000	186	69	10010110	218	64	00100110	250	88	00010001
155	11	10001000	187	D3	11001011	219	C9	10010011	251	10	00001000
156	22	01000100	188	A6	01100101	220	92	01001001	252	20	00000100
157	45	10100010	189	4D	10110010	221	24	00100100	253	40	00000010
158	8B	11010001	190	9A	01011001	222	49	10010010	254	80	00000001
159	17	11101000	191	35	10101100	223	93	11001001	---	--	-----

HEX: Hexadecimal value  
 BIN: Binary value, bit order 0 - 7



**Fig. 14: Captured picture with active 8bit LFSR**

**Example: VHDL Code**

```

signal REG: STD_LOGIC_VECTOR (7 downto 0);
signal DATAIN: STD_LOGIC;

SR8R: process (ICLK)          -- 8 bit LFSR
begin
  if (ICLK'event and ICLK='1') then
    if (RESET = '1') then    -- reset: shift register is loaded with 1
      REG <= "00000001";
    else
      REG <= REG(6 downto 0) & DATAIN;
    end if;
  end if;
end process SR8R;

DATAIN  <= REG(0) xor REG(6);
LFSR_OUT <= REG;

```

19 Appendix G – CE Compliance Statement



# CE Compliance Statement

We,

**Photonfocus AG,**

**8853 Lachen, Schweiz**

declare under our sole responsibility that the following products:

- Megapixel:**      **MV-D1024-28-CL-10**  
                          **MV-D1024-80-CL-8**  
                          **MV-D1024-160-CL-8**
  
- Multiline:**      **MV-D1024x128-28-CL-10**  
                          **MV-D1024x128-80-CL-8**  
                          **MV-D1024x128-160-CL-8**
  
- CCIR:**            **MV-D752-28-CL-10**  
                          **MV-D752-80-CL-8**  
                          **MV-D752-160-CL-8**
  
- VGA:**             **MV-D640-33-CL-10**  
                          **MV-D640-66-CL-10**  
                          **MV-D640-48-U2-10**  
                          **MV-D640C-33-CL-10**  
                          **MV-D640C-66-CL-10**  
                          **MV-D640C-48-U2-10**
  
- Digipeater:**      **CLB26**

are in compliance with the below mentioned standards according to the provisions of „European Standards“ Directive:

- EN 61 000 – 6 – 3 : 2001**
- EN 61 000 – 6 – 2 : 2001**
- EN 61 000 – 4 – 6 : 1996**
- EN 61 000 – 4 – 4 : 1996**
- EN 61 000 – 4 – 3 : 1996**
- EN 61 000 – 4 – 2 : 1995**
- EN 55 022 : 1994**



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Dr. Peter Mario Schwider  
CTO

July 20, 2004

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[CLO2000] Specifications of the Camera Link Interface Standard for Digital Cameras and Frame Grabbers, October 2000

[LOM2000] LVDS Owner's Manual, A General Design Guide for National's Low Voltage Differential Signaling (LVDS) and Bus LVDS Products, 2 nd Edition Spring 2000 National Semiconductor

[MB2002] Microbench system from the LINOS AG, [www.linos.de/en/index.php](http://www.linos.de/en/index.php)

[SOFT] Software manual Photonfocus API software

[PFREMOTE] Software manual Photonfocus graphical user interface PFRemote

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## 23 Revisions and State of Product development

### 23.1 Revisions

**Table 41: Document revisions**

REV	Changes	Date
1.0	First edition	30/07/03
1.1	CE Compliance Statement integrated	28/07/04

**23.2 State of Product development**

Table 42 shows the correlation between camera firmware revision (camera serial number), software revision and revision of the user manual. This table indicates firmware documents and software revisions.

**Table 42: Correlation between firmware, software and user manual**

correlating serial numbers	firmware revision	software revision	document revision	remark
	1.0	0.5	1.0	Freeze camera

## **24 Service information**

### **24.1 Contact for product enquiries and quotations**

For product enquiries and quotations, please contact one of our distributors in your area. A list of distributors can be found at:

[www.photonfocus.com](http://www.photonfocus.com)

### **24.2 Product information, documentation and software updates**

[www.photonfocus.com](http://www.photonfocus.com)

### **24.3 Storage and Transport**

During storage and transport, the camera should be protected against vibration, shock, moisture and dust. The original packing protects the camera adequately from vibration and shock during storage and transport. Please either retain this packing for possible later use or dispose of it according to local regulations.

### **24.4 Preparing for use**

Remove the camera from its packing and ensure that it is complete and undamaged. If any damage has occurred during transport, please immediately contact the transport company and your distributor.

The camera is delivered with a 3-pole power plug. Ensuring that the maximum operating voltage is not exceeded, connect the camera to a suitable power supply. Install the software supplied and test the camera with the PF-Remote program.

### **24.5 Mounting the lens**

Remove the protective cap from the C-mount thread of the camera and screw in the objective. When removing the protective cap or changing the objective, the camera should always be held with the opening facing downwards to prevent dust from the surroundings falling onto the CMOS sensor. If the objective is removed, the protective cap should be refitted.

If the camera is operated in dusty surroundings, we recommend the use of a constant stream of clean air at the front of the objective.

## 25 Guarantee conditions

### Guarantee claims

The manufacturer alone reserves the right to recognize guarantee claims. The guarantee will be rendered null and void in the event of unauthorized manipulation, mechanical damage or damage arising from inappropriate use or from mechanical or electrical modifications, especially soldering. The guarantee will also be invalidated if the apparatus is used for purposes for which it was not designed, if it is incorrectly connected or if it is not used according to the operating instructions.

### Guarantee work

can only be assured and carried out by the manufacturer.

### Repair time

will normally be a maximum of 10 working days for repairs to a device for which a legitimate guarantee claim is made.

### Claims for damages

of all kinds, especially those arising from use, are excluded. Liability is limited, in all cases, to the value of our product.

### In case of damage

If the equipment is defective, return it, in the original packing and with a copy of the receipt, to the following address:

**Photonfocus AG  
Bahnhofplatz 10  
CH-8853 Lachen**

Important: Include a written description of the fault as well as your full postal address. The equipment will be forwarded in your name to the service department and, in the event of a legitimate guarantee claim, returned to you without freight charges.

### Safety hints

The apparatus conforms with approved electro-magnetic standards. Opening the apparatus is not permitted. Furthermore, all guarantee claims will be invalidated by inappropriate use. In all circumstances, the following should be noted:

- The apparatus may only be used for the purpose described.
- The apparatus is only suitable for indoor use. Protect it from moisture and heat.
- The permitted operating temperature range is 0°C to 60°C.
- Never attempt repairs yourself. Repairs may only be carried out by trained expert staff.
- Moreover, every piece of equipment is tested before delivery and has a guarantee symbol attached.
- For cleaning purpose, use only a dry soft cloth. Never use water or chemicals.